3D RAGE™ PRO
Graphics Controller Specifications

Technical Reference Manual
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Record of Revisions

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2.01	June 97	Second Release Final
2.02	Aug. 97	Release
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Technical Reference Manuals

3D RAGE PRO series

- 3D RAGE PRO™ Register Reference Guide (RRG-GO3500)
- 3D RAGE PRO™ Graphics Controller Specifications (GCS-C03500)

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Chapter 1
Introduction

1.1 About This Manual

This manual is part of a set of reference documents which provide information necessary to design the *3D RAGE PRO* into a graphics subsystem. These documents are listed in the System Publications Index at the beginning of this manual.

The electrical and thermal characteristics described in this document are specific to the *3D RAGE PRO* manufactured using UMC's 0.35µm process — which has voltages of 3.3V core, 5.0V PCI I/O, 3.3V AGP, and 3.3V memory interface. Please contact ATI to obtain information on how to support all of ATI's graphics controllers, steppings, and foundries in one PCB design.

1.2 Conventions

1.2.1 Mnemonics

Mnemonics are used throughout this manual in place of external strap pin resistor names and signal names. Active-low signal names are identified by the # character.

The following example is the mnemonic for the VFC Sense strap signal:

VFC_SENSE#

The example below refers to the Product Type Code field that occupies bit positions 0 through 15 within the 16-bit vendor ID register in PCI configuration space:

SUBSYS_VEN_ID[15:0]

1.2.2 Numeric Representation

Hexadecimal numbers are appended with "h" (Intel assembly-style notation) whenever there is a risk of ambiguity. Other numbers are assumed to be in decimal.

Several signals of identical function are sometimes described by a single expression in which the part of the signal name that differs is shown in parenthesis ( ). For example, the four Select signals — SEL#0, SEL#1, SEL#2, and SEL#3 — are represented by the single expression SEL#(0:3).

1.2.3 Acronyms

Standard acronyms used in the literature are presumed known and will not be explained. When in doubt, the reader can refer to the following table for a quick check. Less frequently used or ATI-specific acronyms will have the full definition alongside in parenthesis when they appear the first time in the document.

Table 1-1 Standard Acronyms

Acronym	Full Expression
AGP	Accelerated Graphics Port
ALU	Arithmetic Logic Unit
AMC	ATI Multimedia Channel
BGA	Ball Grid Array
CRC	Cyclic redundancy check
DVS	Digital Video System
EPROM	Erasable Programmable Read Only Memory
FIFO	First In, First Out
I^2C	Bus Protocol (Philips Specification)
MDP	MPEG Data Port
MPP	Multimedia Peripheral Port
PEROM	Flash Programmable and Erasable Read Only Memory
PQFP	Plastic Quad Flat Pack
UV	Chrominance (also CrCb). Corresponds to the color of an image pixel.
VBI	Vertical Blank Interval
VFC	VGA Feature Connector
YUV	The method of video signal color encoding. Includes luminance (Y, black and white component) and chrominance (UV, color component)

Chapter 2
Overview

The *3D RAGE PRO* Graphics Accelerator sets the standard on 2D/3D and video performance for the new generation of AGP graphics accelerators. Designed to take full advantage of Intel's AGP (Accelerated Graphics Port) high-speed interface, *3D RAGE PRO* features 100MHz SGRAM or WRAM memory support, floating-point set-up engine, 4K texture cache, a host of unique 3D features, 230MHz DAC and enhanced MPEG-2 motion compensation. The *3D RAGE PRO* is the industry's first accelerator to unleash the full potential of AGP for advanced processors such as the Pentium II.

2.1 Unique Features

2.1.1 AGP 2X mode

Unlike competing solutions, which use AGP 1X mode only, the DVD-enabled *3D RAGE PRO AGP 2X*, with three times the 3D performance of the previous generation chip, is the first demonstrated AGP accelerator to support the AGP 2X (133MHz) mode. The AGP 2X mode offers a peak bandwidth in excess of 500 MB/s, which is twice the throughput of the AGP 1X (66MHz) mode. The PCI graphics devices are limited to a 33MB/s bandwidth which must be shared with other PCI devices. The *3D RAGE PRO* also supports AGP's pipeline and sideband protocols. These significantly improve the sustained bandwidth that is critical to the enhanced 3D and video performance.

2.1.2 Floating-Point Set-up Engine

The *3D RAGE PRO* integrates a floating-point set-up engine capable of processing up to 1.2 million triangles per second. By off-loading the set-up function from the CPU, allowing it to focus on 3D geometry and lighting transformations, the *3D RAGE PRO* dramatically improves the performance of the entire 3D pipeline.

Compared with competing first generation set-up engines which only accept fixed-point parameters, requiring the CPU to perform float-to-fixed conversions that can take up to 100 CPU clocks, ATI's floating point architecture opens the door to the highest level of 3D performance.

2.1.3 100 MHz SGRAM

Frame buffer bandwidth is another important factor affecting 3D and 2D graphics performance. *3D RAGE PRO*'s 64-bit, 100MHz SGRAM interface delivers 800 MB/s of low-latency frame buffer bandwidth, the highest achieved by any mainstream graphics controller.

It is the ideal complement to the high bandwidth AGP 2X mode interface. By contrast, single-channel, non-concurrent RAMBUS designs used by others are limited to 600 MB/s of high-latency bandwidth.

ATI can provide design assistance, including IBIS models, to allow OEMs to design 100MHz memory upgrades on motherboards using the new industry standard SGRAM SO-DIMMs.

2.1.4 DVD and Video Support

DVD and video features include enhanced motion compensation acceleration and a 4-tap horizontal and 2-tap vertical high quality DVD video scaler, providing smooth images without the "jaggies" (jagged edges) common to today's video products. The scaler provides true color video display, independent of the graphics mode used.

3D RAGE PRO also features a de-interlacing filter, video on graphics overlay, multi-stream video, color-space conversion, scatter-gather bus-master, planar YUV mode, ATI Multimedia Channel (AMC) video input port and support for high quality NTSC and PAL TV-out with the ATI ImpacTV chip.

By off-loading the motion compensation step from an MMX processor, *3D RAGE PRO* improves software DVD/MPEG-2 frame rate by 20 to 30%. *3D RAGE PRO* provides full motion MPEG-2 playback on Pentium II processors, without the need for DVD hardware.

2.2 Feature List

2.2.1 General Features

- High integration results in a low cost, small footprint graphics subsystem, ideal for motherboard designs.
- PCI version 2.1 with full bus mastering and scatter/gather support.
- Bi-endian support for compliance on a variety of processor platforms.
- Fast response to host commands:
  - 128-level command FIFO
  - 32-bit wide memory-mapped registers
  - Programmable flat or paged memory model with linear frame buffer access
- Triple 8-bit palette DAC with gamma correction for true WYSIWYG color. Pixel rates up to 230MHz.
- Supports DRAM, EDO DRAM, SDRAM and SGRAM at up to 100MHz memory

clock providing bandwidths up to 800MB/sec across a 64-bit interface.

- Supports WRAM and 128-bit external DAC for ultra-high end configurations.
- Flexible graphics memory configurations: 2MB up to 8MB EDO/SDRAM/SGRAM, 4MB to 16MB WRAM.
- Memory upgrade via industry standard SGRAM SO-DIMM, for reduced board area and higher memory speeds.
- DDC1 and DDC2B+ for Plug-and-Play monitors.
- Power management with full VESA DPMS and EPA Energy Star compliance.
- Integrated hardware diagnostic tests performed automatically upon initialization.
- High quality components through built-in SCAN, Iddq, CRC and chip diagnostics.
- Single chip solution in 0.35µm, 3.3V CMOS technology, with multiple package options.
- Comprehensive HDKs, SDKs and utilities augmented by full engineering support.
- Complete local language supports (contact ATI for current list).

2.2.2 2D Acceleration

- Hardware acceleration of Bitblt, Line Draw, Polygon / Rectangle Fill, Bit Masking, Monochrome Expansion, Panning/Scrolling, Scissoring, full ROP support and h/w cursor (up to 64x64x2).
- Game acceleration (including support for Microsoft's DirectDraw): Double Buffering, Virtual Sprites, Transparent Blit, Masked Blit and Context Chaining.
- Acceleration in 8/16/24/32 bpp modes. Packed pixel support (24bpp) enables true color in 1MB configurations.

2.2.3 3D Acceleration

- Integrated 1 million triangle/s set-up engine reduces CPU and bus bandwidth requirements and dramatically improves performance of small 3D primitives
- 4K on-chip texture cache dramatically improves large triangle performance.
- Complete 3D primitive support: points, lines, triangles, lists, strips and quadrilaterals and BLTs with Z compare.
- Comprehensive enhanced 3D feature set:
  - Full screen or window double buffering for smooth animation
  - Hidden surface removal using 16-bit Z-buffering

- Edge anti-aliasing
- Sub-pixel and sub-texel accuracy
- Gouraud and specular shaded polygons
- Perspectively correct mip-mapped texturing with chroma-key support
- Support for single pass bi- and tri-linear texture filtering, vastly improving bi- and trilinear performance
- Full support for Direct3D texture lighting
- Texture compositing
- Special effects such as complete alpha blending, fog, video textures, texture lighting, reflections, shadows, spotlights, LOD biasing and texture morphing
- Dithering support in 16bpp for near 24bpp quality in less memory
- Texture compression of up to 8:1 using vector quantization

- Extensive 3D mode support:
  - Draw in RGBA32, RGBA16, and RGB16
  - Texture map modes: RGBA32, RGBA16, RGB16, RGB8, ARGB4444, YUV444
  - Compressed texture modes: YUV422, CLUT4 (CI4), CLUT8 (CI8), VQ

2.2.4 Motion Video Acceleration

- Smooth video scaling and enhanced YUV to RGB color space conversion for full-screen / full-speed video playback.
- Front and back end scalers support multi-stream video for video conferencing and other applications.
- Filtered horizontal/vertical, up/down scaling enhances playback quality.
- Enhanced line buffer allows vertical filtering of native MPEG-2 size (720x480) images.
- DVD / MPEG-2 decode assist provides dramatically improved frame rate without incurring cost of dedicated hardware.
- Special filter circuitry eliminates video artifacts caused by displaying interlaced video on non-interlaced displays.
- Bi-directional bus mastering engine with planar YUV to packed format converter for superior MPEG-2 and video conferencing.
- Hardware mirroring for flipping video images in video conferencing systems.
- Supports graphics and video keying for effective overlay of video and graphics.

- YUV to RGB color space converter with support for both packed and planar YUV:
  - YUV422, YUV410, YUV420
  - RGB32, RGB16/15, RGB8, Mono

2.2.5 AMC Operation

- 16-bit, bi-directional video port allows direct connection to popular video upgrades such as:
  - Video capture / video conferencing
  - Hardware MPEG-2 / DVD player
  - TV Tuner with Intercast support
  - Interface to ATI's ImpacTV chip

2.3 Product Family

2.3.1 Chip Packaging Options

The *3D RAGE PRO* is available in five AGP and PCI packaging options with different levels of AGP support, giving manufacturers maximum flexibility to differentiate products and upgrade existing design. The table below indicates the several configurations in which the 3D RAGE PRO is available.

Table 2-1 3D RAGE PRO packaging and identification codes

Chip ID	Description
GB	BGA package, AGP: both 1X and 2X
GD	BGA package, AGP: 1X support only
GI	BGA package, PCI 33MHz only
GP	PQFP package, PCI 33MHz

3D RAGE PRO AGP 2X

- Incorporates AGP 2X mode (133MHz) and 230MHz DAC support
- Triple 8-bit palette DAC supporting pixel rates up to 230MHz
- Available in 256-pin BGA for optimal electrical characteristics in the demanding AGP environment.

3D RAGE PRO AGP 1X

- Incorporates AGP 1X (66MHz) support with pipelining and sideband address support.
- Triple 8-bit palette DAC supporting pixel rates up to 200MHz
- Available in 256-pin BGA package. This is a pin-compatible alternative to *3D RAGE PRO AGP 2X* for cost-sensitive implementations.

3D RAGE PRO PCI

- Incorporates 33MHz PCI revision 2.1 support.

Available in 208-pin PQFP package and pin-compatible with *3D RAGE II /II+*. An ideal upgrade to extend the life of existing motherboards, and the most economical solution for non-AGP systems, the PCI version incorporates the same performance enhancements and new features found in the AGP *3D RAGE PRO* versions.

2.3.2 Add-on Cards

ATI Multimedia Channel (AMC) add-on cards for *3D RAGE PRO* include ATI's existing line of TV tuners, video capture and hardware DVD/MPEG-2.

2.4 Software Support

Table 2-2 Workstation Class / Arcade Level 3D Accelerator

Software Support	DOS	Win 3.x	Win 95	Win NT	Mac OS	OS/2
2D Software Support [1]						
Accelerated driver support	VESA[2]	*	*	*	*	*
AutoCAD / MicroStation						
Video Software Support						
Microsoft DirectDraw			*			
Microsoft ActiveMovie			*			
MPEG-1 software playback	*	*	*			
MPEG-2 software playback			*			
3D Software Support						
Microsoft Direct3D			*			
QuickDraw 3D RAVE			*	*	*	
OpenGL[3]			*	*		
Heidi				*		
ATI 3D CIF[4]			*			

1 - Additional 3rd parties (including SCO Unix and UNIXWARE);
2 - Direct BIOS support;

3 - Includes NT 3.51ICD and NT4.0 MCD;
4 - ATI's 3D API for the 3D RAGE family

2.5 Market Orientation

2.5.1 Corporate PC Market

ATI designed the *3D RAGE PRO* to be the ideal corporate PC accelerator, with the performance, reliability, and software support that corporate users demand today along with the 3D features and performance needed to use the upcoming wave of corporate 3D applications.

3D RAGE PRO is available with an integrated 230MHz DAC that supports 1600x1200 resolution at the 85Hz refresh rate specified by the European market. Industry-leading 2D performance is provided by 100MHz SGRAM, faster 2D engine speed, a deeper command FIFO, AGP 2X mode and optimized drivers.

For PC workstations, the *3D RAGE PRO* can be configured with WRAM memory and an external 250MHz DAC that will provide unmatched 2D and 3D performance at high resolutions and color depths. *3D RAGE PRO* is the first mainstream part to incorporate edge anti-aliasing, deemed a necessity by CAD users.

Drivers are available for all corporate operating systems and API's (see section 2.4), including Windows NT 4.0/5.0, Windows 95, Memphis, OS/2, Mac OS, DirectX, Open GL, Heidi and QuickDraw3D. This allows support for 3D applications such as SGI's Cosmo Player VRML 2.0 browser, which will be bundled with ATI products.

2.5.2 Consumer PC Market

With games in mind, ATI has enhanced the 3D performance of the *3D RAGE PRO* by a factor of three over the previous generation chip. In addition, the *3D RAGE PRO* incorporates advanced 3D features to allow greater realism. These include texture compositing, single pass trilinear filtering, specular highlights, video textures and VQ (vector quantization) texture decompression.

In AGP 2X mode, fast direct access to large amounts of main memory allows for large textures, which result in much greater graphical detail. The 4KB on-chip texture cache reduces the memory bandwidth requirements and latency, providing benefits in either AGP or PCI modes.

With a rendering engine capable of 1.2 million triangles/second and a peak fill rates of 75 million textured pixels/second, the *3D RAGE PRO* surpasses even high-end 3D game add-in boards on the market today.

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Chapter 3
Functional Description

The *3D RAGE PRO* controller comprises several major subsystems and interfaces as shown in the figure below. This chapter describes them briefly from a functional point of view.

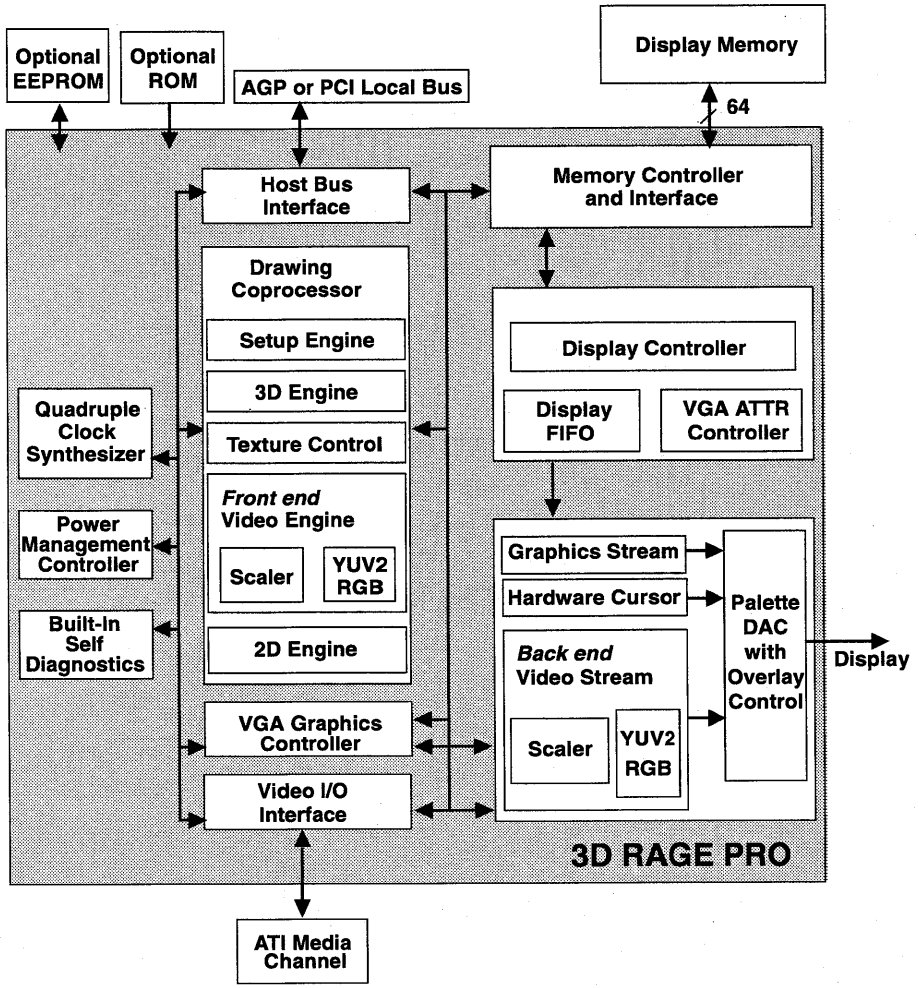

Figure 3-1. 3D RAGE PRO Functional Block Diagram

3.1 3D Graphics Coprocessor

The 3D graphics coprocessor offers a number of orthogonal pixel processing features associated with the rendering of 3D images. These coprocessor functions were chosen to accelerate features of both Microsoft's D3D and Apple's QuickDraw 3D RAVE interfaces. Drivers will be available for all major operating systems and APIs (see Section 2.5).

The *3D RAGE PRO* graphics processor includes a triangle setup engine, which needs only color, alpha, Z, U and V information at vertices of triangles to successfully draw Gouraud shaded, or perspectively correct texture mapped triangles. The setup engine significantly reduces the CPUs load in 3D graphics applications, giving applications more CPU time to perform non-setup related tasks.

Pixels to be displayed can be further modified by alpha blending with pixels in the destination, by fogging pixels with a fog color, and in the case of texture mapping, by lighting them. Depth buffering is achieved by associating a 16-bit Z value with each pixel. The Z, alpha, and fog color for each new pixel is supplied from interpolators within the 3D coprocessor. In case of texture mapping, the alpha factor may even be stored in the texture map on a pixel-by-pixel basis.

Pixels in the 3D coprocessor are always operated on as 24-bit entities (8 bits each of Red, Green, and Blue). Other pixel sizes, i.e., 8-bit and 16-bit, are dithered by the 3D graphics subsystem to output at the desired pixel size.

The 3D coprocessor contains a powerful texture mapping engine. This engine takes a series of precomputed maps (mip maps) and selects texels from these maps in a way that allows them to look perspectively correct. Texels can be filtered in a number of ways, and then lit (lightened or darkened). Once the texel is formed by filtering and lighting, any of the pixel processing modes mentioned previously can be applied to the texel.

A newly added 4K texture cache greatly reduces the memory bandwidth needed to support texture mapping.

With AGP support, texture maps can be stored in system memory and pulled into the local texture cache as needed. This rids the system of the need to add significant amount of local frame buffer memory in order to support multiple detailed texture maps, and allows applications to support a richer and more realistic environment.

3.2 2D Engine

The is a fixed-function subunit that runs concurrently to the host processor. It is dedicated to draw operations which include rectangle fill, line draw, polygon boundary lines, and polygon fill. A sophisticated pixel data path allows monochrome-to-two-color expansion,

solid color fill, screen-to-screen bitblts, fixed pattern fill, general pattern fill, general patterns with rotation, and host-to-screen data transfers. Flexible bitblt trajectories allow hyper-efficient off-screen memory management, effectively increasing bitmap and font cache sizes and improving performance.

Other features include GUI engine quick setup which off-loads draw engine setup from the host CPU. A 16-function ALU and a four-function source/destination color comparator allow source and destination to be combined in a multitude of ways, useful for operations such as image overlaying or transparent blits. Bit masking and scissoring can protect memory regions from being written.

All internal draw engine data paths are 64-bit wide. Full drawing features are available in 8, 15, 16, 24, and 32 bits-per-pixel (bpp) modes.

All draw engine registers are 32-bit wide. A 128x32 command FIFO improves throughput over the expansion bus. Additional 64 entries are dedicated to busmastering16x64 source and destination FIFOs improving memory bandwidth throughput.

3.3 Video Coprocessor

The video coprocessor has an optimized data path designed for scaling, filtering, and color space conversion. Dual 768-pixel line buffer has been integrated into this block to provide superior vertical scaling and interpolation. Graphics and video keying capabilities and a window controller allow for overlaying of the graphics and video data streams. This enables simultaneous display of 24bpp video and 8/16/24/32bpp graphics.

3.4 Host Bus Interface

The Host Bus Interface supports both AGP and PCI 2.1 standards. Support for AGP includes both sideband and mixed address modes. Texture map data for 3D objects can be obtained directly from system memory. Similarly the AGP can be used to accumulate MPEG-2 playback.

With PCI 2.1, functions such as bus control, data flow control, address/data signal generation, signal timings, and address decoding are supported. Data flow control is enhanced by a 6x64-bit write-through FIFO available in both VGA and direct memory modes.

Bus mastering functions between (1) system memory and frame buffer, (2) system memory and MPP, and (3) system memory and GUI engine, allow all data transfer operations to be off-loaded from the host processor onto the motherboard chip set.

3.5 Memory Controller and Interface

The memory controller subsystem arbitrates requests from the direct memory interface, the VGA graphics controller, the drawing coprocessor, the display controller, the video scaler, and the hardware cursor. Requests are serviced in a manner that ensures display integrity and maximum CPU/coprocessor drawing performance.

A dedicated DRAM frame buffer can be 2MB or 4MB in size using Fast Page or EDO DRAM. A dedicated synchronous DRAM frame buffer can be 2MB, 4MB, or 8MB in size using SDRAM or SGRAM. A dedicated WRAM frame buffer can be 8MB or 16MB in size.

Table 3-1 Memory Controller

Memory Type	2MB	4MB	8MB	16MB
DRAM, EDO DRAM	-	-	-	-
	256Kx8	-	-	-
	256Kx16	256Kx16	-	-
SDRAM, SGRAM	128Kx16x2	128Kx16x2	-	-
	128Kx32x2	128Kx32x2	-	-
	256Kx32x2	256Kx32x2	256Kx32x2	-
WRAM	-	256Kx32	256Kx32	256Kx32

3.6 Extended VGA Graphics Controller

The VGA portion of the graphics controller is fully register compatible with the VGA standard and is BIOS-compatible with VESA super VGA drivers.

3.7 CRT Controller (CRTC)

The CRTC subsystem has additional enhancements such as support for overscan, video memory sizes up to 8MB, and screen resolutions up to 1600x1200 non-interlaced.

3.8 Display Controller

The display controller subsystem consists of four subunits as follows:

- Display FIFO to manage the memory interface for displayed pixel data.
- Enhanced attribute controller for VGA.
- The display controller.
- 128 bit external RAMDAC supported with WRAM.

This display controller subsystem supports VGA graphics modes up to 1600x1200 (85Hz), VGA text modes up to 132-column on a PS/2 monitor, and accelerator display modes up to 1600x1200 (85Hz).

3.9 Palette DAC

The internal palette DAC subsystem consists of a triple 256x8 SRAM palette and a triple 8-bit DAC. It supports the following features:

- Pixel clock rates up to 230MHz for resolutions up to 1600x1200.
- Refresh rates up to 200Hz.
- Built-in DAC reference generation.
- Monitor detection.
- Direct 24-bit color.
- Separate or composite horizontal and vertical Sync signals.
- Optimized slew rate control for the RGB analog output for low EMI emission.

3.10 Quadruple Clock Synthesizer

The internal clock synthesizer consists of four independent phase locked loops (PLL) capable of synthesizing any frequency up to 230MHz. All PLLs have been optimized for low jitter graphics applications.

- The first PLL generates clocks for the CRTC, display controller, and palette DAC. This PLL can be reprogrammed by the BIOS for each display mode.
- The second PLL generates the clock for the drawing coprocessor.
- The third PLL is used to generate the 66 MHz and 133 MHz internal clock synchronous AGP bus operations.
- The fourth PLL generates the clock for the memory controller.

3.11 Hardware Cursor

The hardware cursor logic supports a 64x64x2 memory-mapped cursor that is also XGA function compatible. The hardware cursor may be used in any display mode supported by this controller. Transparent, complement, and two solid colors are available.

3.12 ATI Multimedia Channel (AMC)

The AMC represents a collection of hardware and software components designed to facilitate the use of ATI products for multimedia applications. It consists of a non-chip audio bus, and three ports into the graphics controller - the DVS port for video input into the graphics controller, the MPP port for video input and output from the graphics controller, and the I^2C port for controlling attached devices. It is backward compatible with the VFC interface.

The Multimedia Peripheral Port (MPP) Mode supported by AMC allows interface with external I/O devices. For example, compressed data can be transferred by means of MPP from the host (CPU) to the MPEG-2 decoder for DVD applications.

Display data can also be streamed out from *3D RAGE PRO* to the device (e.g. TV-Out chip). For such applications, an ATI external encoder, such as ImpacTV, can be attached to generate NTSC/PAL video for a TV-type display.

The Digital Video Stream (DVS) port accepts industry standard video formats, and allows easy attachment of video decoders and hardware MPEG-2 decoders. The DVS port provides for decoded video data to stream back to the graphics controller.

The I^2C is an industry standard serial bus that allows control and programming of a wide range of peripherals. The 3D RAGE PRO incorporates an I^2C interface to allow programming of peripherals such as video decoders, TV tuners, teletext decoders, and volume control.

The VGA Feature Connector (VFC) is VESA compatible. The VFC-compatible peripherals can be attached directly to the AMC/VFC port.

The following block diagram depicts the major interfaces required in a typical design based on the *3D RAGE PRO*. These interface blocks are further described in later sections of this chapter. Please note that the interface diagrams are generic. You are invited to refer to the reference schematics for this chip for the latest information.

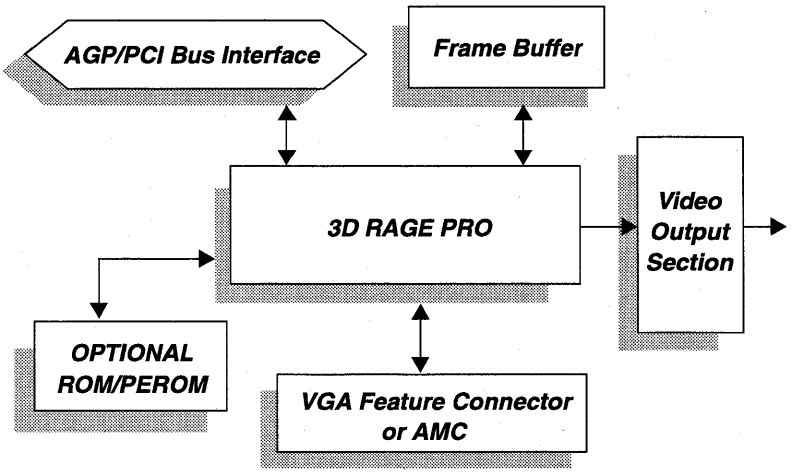

Figure 4-1. Controller Interface

4.1 AGP/PCI Bus Interface

The *3D RAGE PRO* controller supports the Accelerated Graphics Port (both AGP 66MHz and 133MHz). Addressing modes include sideband address support. This AGP enabled controller can access large texture maps, stored in system memory, directly. Applications that make use of large numbers of 3D objects can reduce the amount of memory required in the frame buffer.

Together with PCI Version 2.1, the *3D RAGE PRO* controller acts as a target device, supporting 32-bit memory and I/O operations and byte lane swapping. With full 32-bit address decoding available in PCI, it can map the Direct Memory Interface to 4GB of memory space on a 16MB boundary.

The controller achieves zero wait-state memory read/write burst cycles with burst access. It also supports Block I/O decoding and DAC palette snooping.

Bus mastering allows data transfer operations without CPU intervention. In bus master mode, the controller will take control of the PCI bus by driving the address and control signals.

AGP Bus Configuration is shown in *Figure 4-2.*

PCI Bus Configuration is shown in *Figure 4-3.*

4.1.1 The AGP Bus Interface

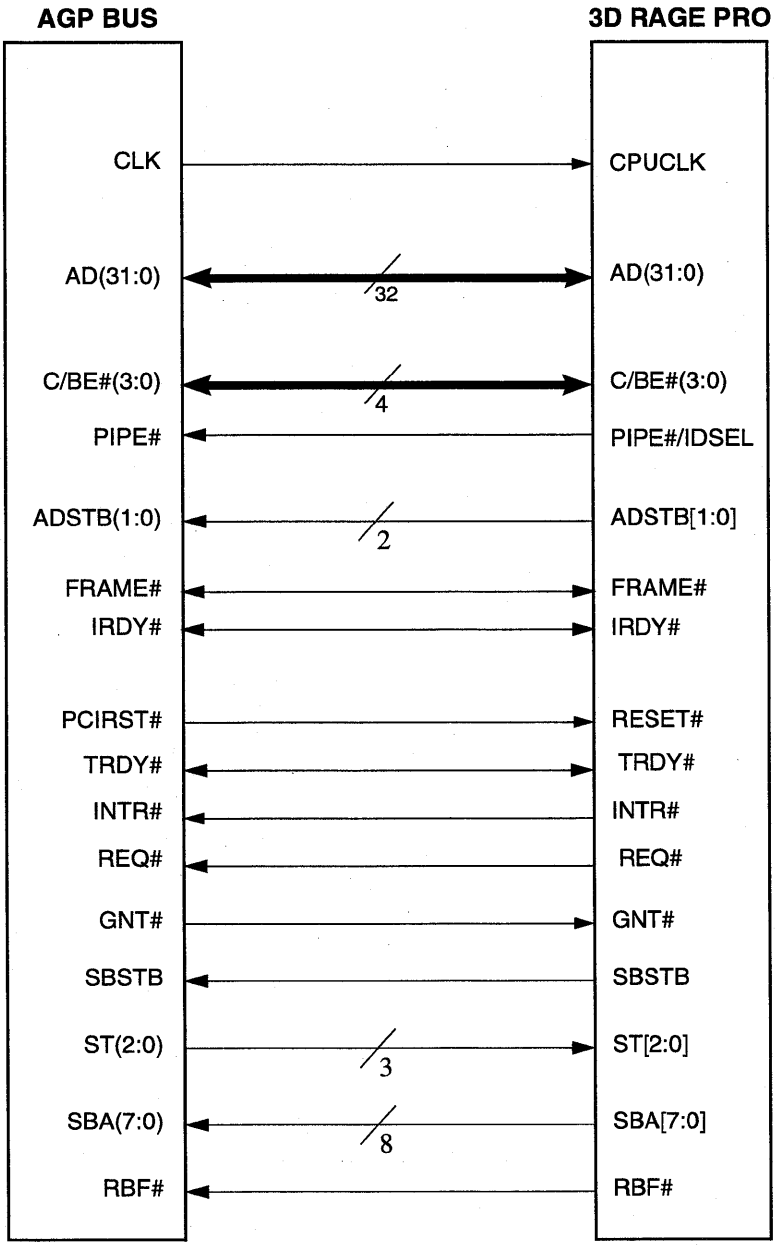

Figure 4-2. AGP Bus Configuration

4.1.2 The PCI Bus Interface

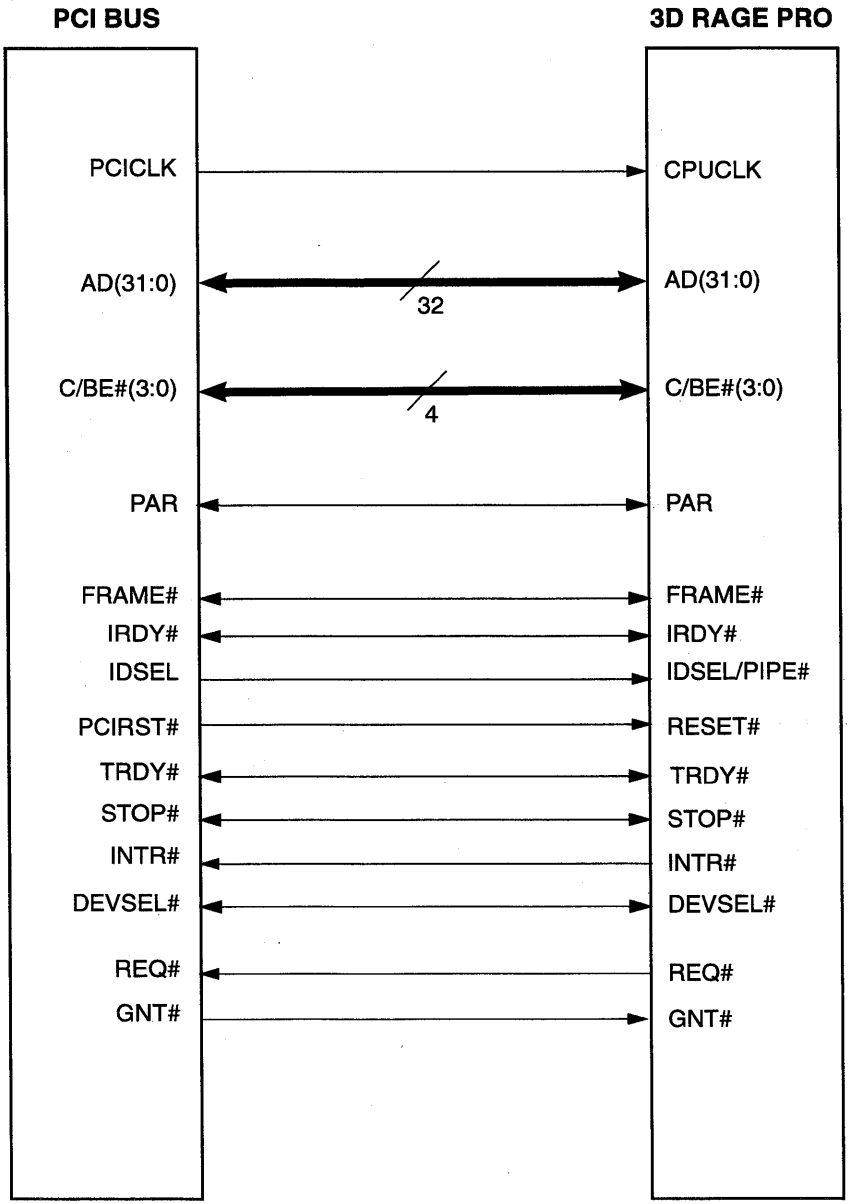

Figure 4-3. PCI Bus Configuration

4.2 Memory Interfaces

The memory interface of this controller supports the following memory devices:

SDRAM, SGRAM and **WRAM** — 128x16x2, 128x32x2, 256x32x2 and 512x32x2.

DRAM and **EDO DRAM** — 256x4, 256x8, and 256x16.

Memory configurations range from 2MB to 8MB (see table below). This interface supports only a full 64-bit memory path.

This interface supports mixing of memory component sizes — 256x4, 256x8, and 256x16 — within one design. However it does not support mixing of memory types, e.g., the mixing of DRAM and EDO DRAM.

The table below lists the supported memory configurations, and the number of memory parts required:

Table 4-1 Memory Interface Support

Memory Size	256x8 (2Mb)	256x16/ 128x16x2 (4Mb)	128x32x2 (8Mb)	256x32x2
2MB	8	4	2	Not supported
4MB	Not recommended	8	4	2
6MB	-	Not recommended	6	-
8MB	-	Not recommended	8	4

Supported memory interface types include "Dual CAS" DRAM, EDO DRAM, WRAM (symmetrical types), SDRAM, and SGRAM devices. Strap resistors are installed on pins MD[48:50] to identify which of these memory types are in use. See Chapter 5, "Controller Configuration", for details on strap resistors usage. This scheme allows your design to support multiple memory implementations using one BIOS.

Figure 4-4 shows a 256x16 Dual CAS memory implementation.

An SDRAM memory implementation example using 128x16x2 SDRAM devices is shown in *Figure 4-5.*

An SGRAM memory implementation example using 128x32x2 SGRAM devices is shown in *Figure 4-6.*

An SGRAM example with 256x32x2 is implemented on *Figure 4-7* SGRAM example using 512x32x2 SGRAM devices is shown in *Figure 4-8.*

Figure 4-9 shows an example of SO-DIMM Module Interface implementation.

Examples of WRAM memory implementation using 256x32 WRAM devices and external DAC interface for WRAM are shown in *Figure 4-10* and *Figure 4-11*.

4.2.1 DRAM Interface

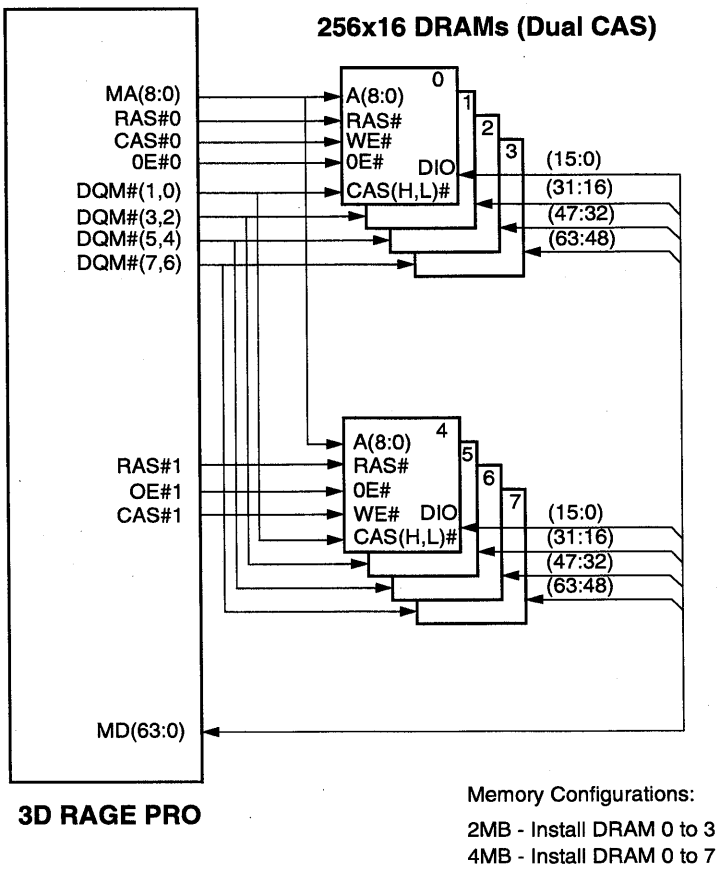

Figure 4-4. DRAM Implementation

4.2.2 SDRAM Interface

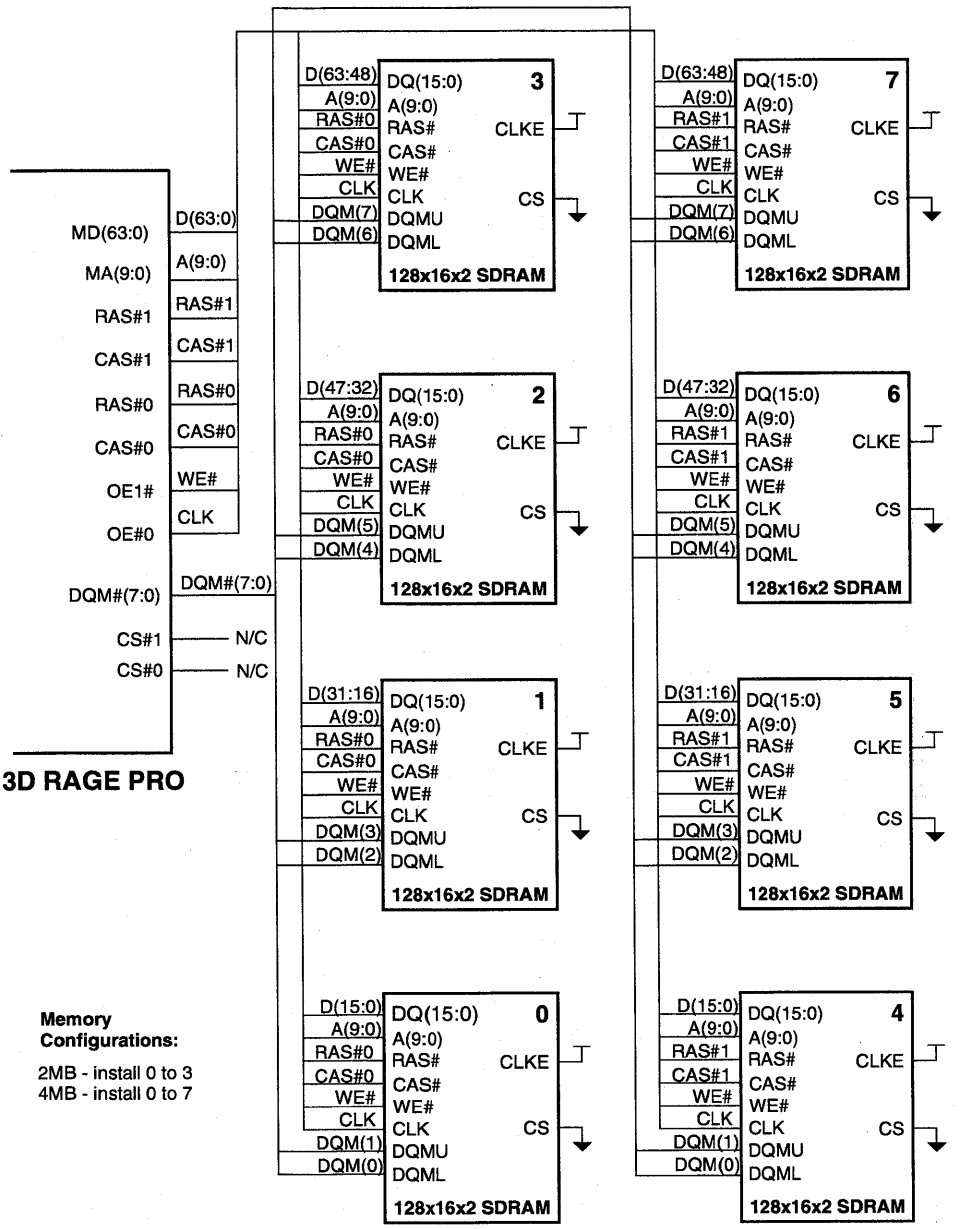

Figure 4-5. SDRAM Implementation

4.2.3 SGRAM Interface with 128x32x2 (8 Mbit) SGRAMs

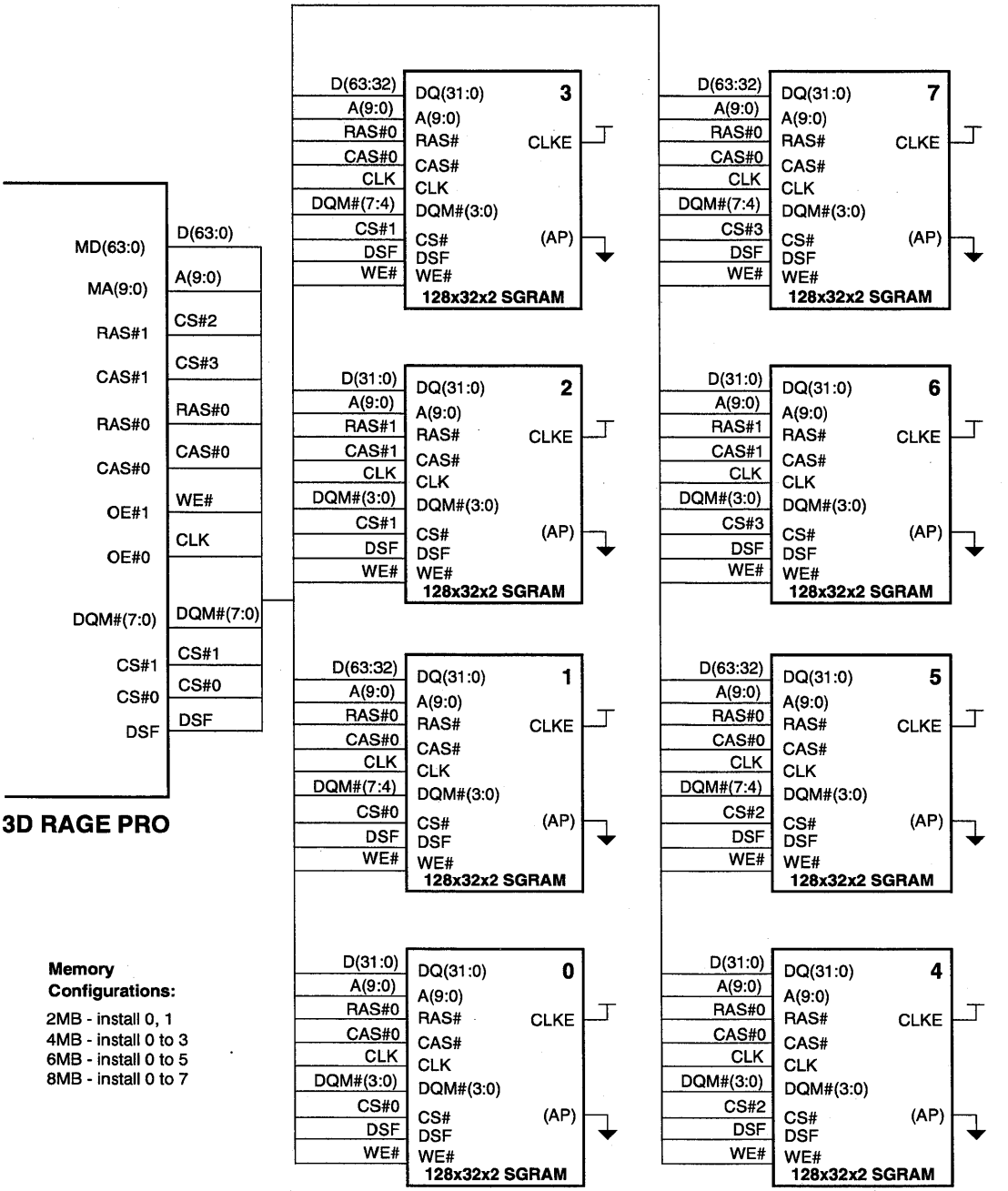

Figure 4-6. SGRAM Implementation (8 Mbit)

4.2.4 SGRAM Interface with 256x32x2 (16 Mbit) SGRAMs

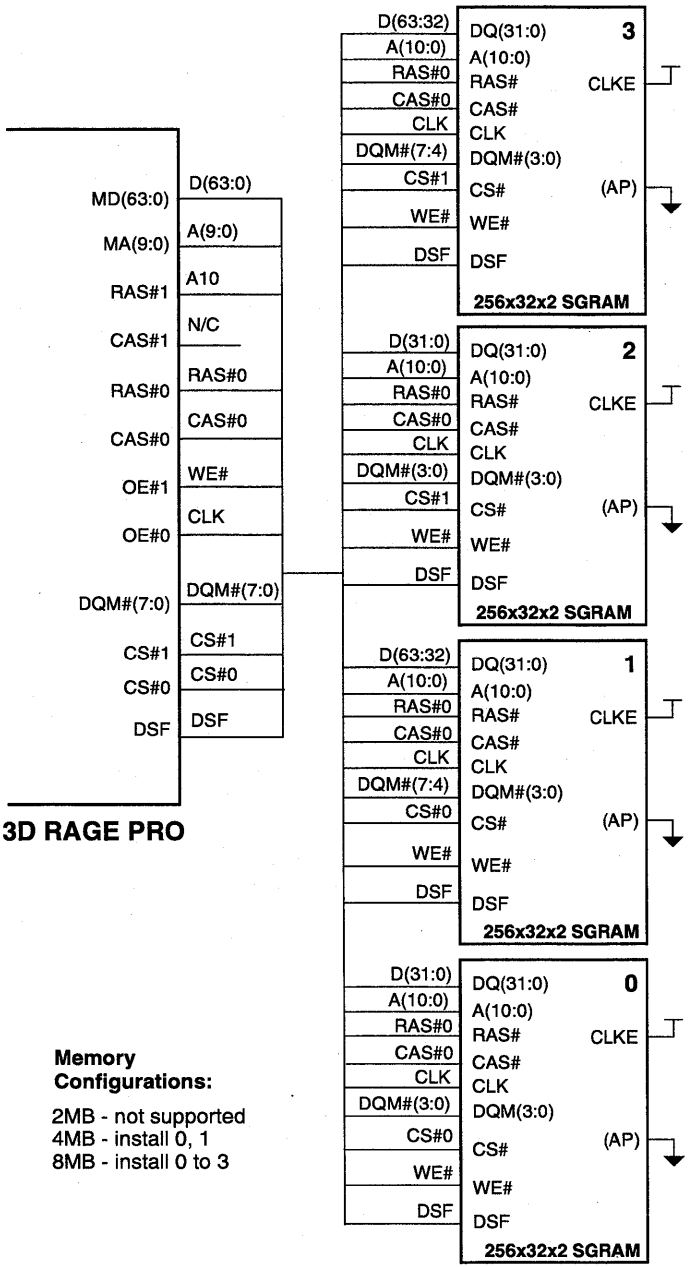

Figure 4-7. SGRAM Implementation (16 Mbit)

4.2.5 SGRAM Interface with 512x32x2 (32 Mbit) SGRAMs

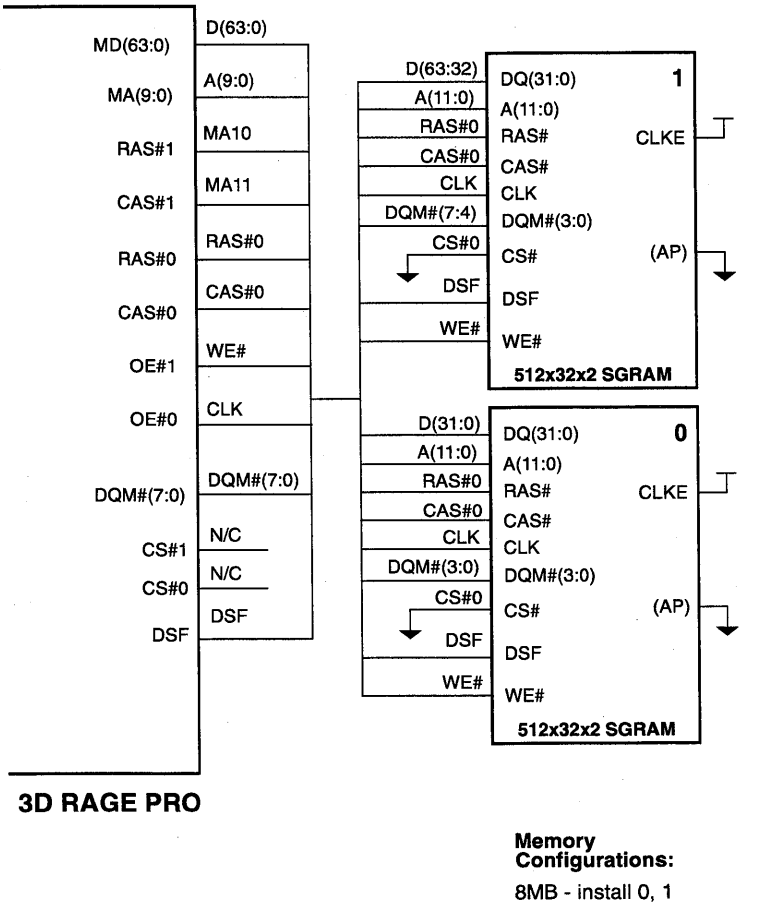

Figure 4-8. SGRAM Implementation (32 Mbit)

4.2.6 SO-DIMM Module Interface

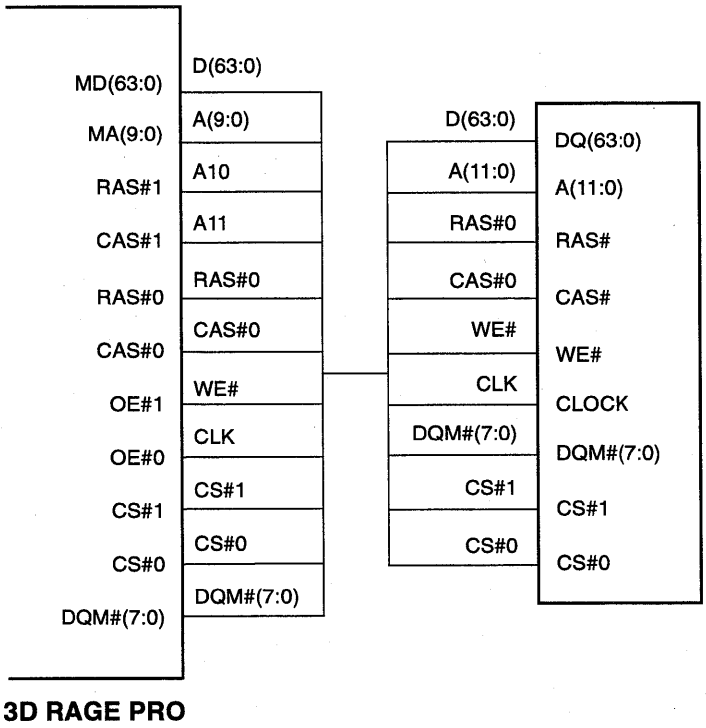

Figure 4-9. SO-DIMM Module Implementation

4.2.7 External DAC Interface for WRAM

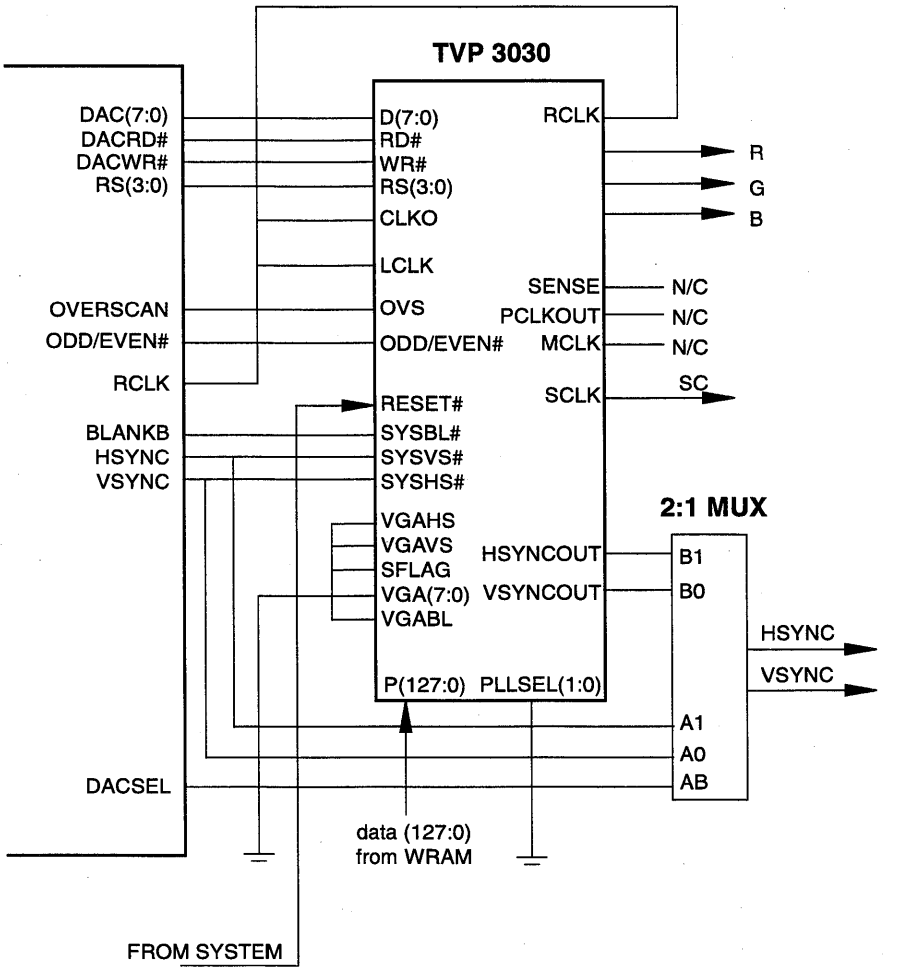

Figure 4-10. External DAC Implementation

4.2.8 WRAM Interface

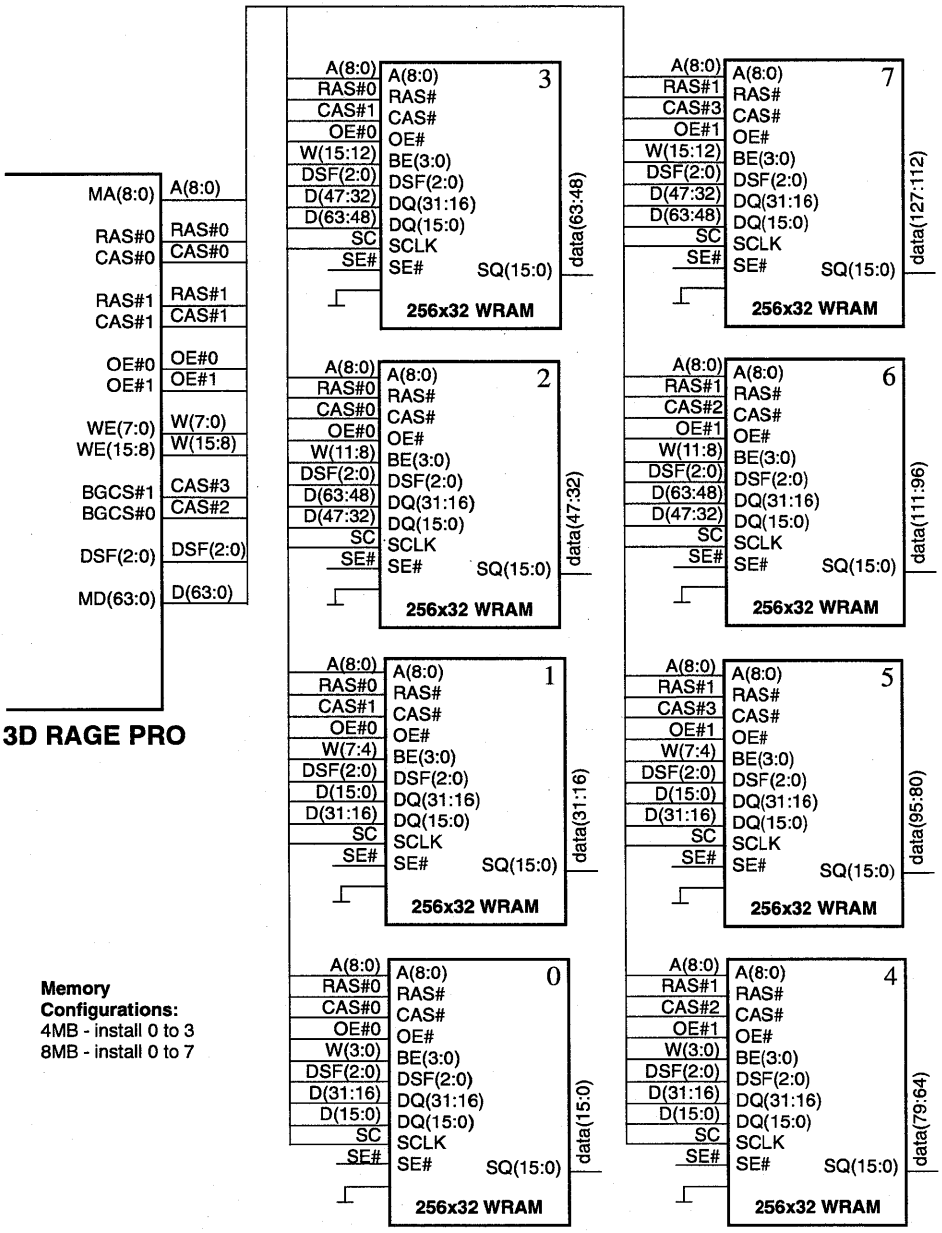

Figure 4-11. WRAM Implementation

4.2.9 EPROM Interface

The video BIOS may be stored in either a 32K or a 64K EPROM (27256/27512), or integrated into the system BIOS. ATI offers a BIOS kit which is used for BIOS customizing or integration of the video BIOS with the system BIOS (see *Figure 4-12*). This kit allows certain BIOS options to be created, for example:

- 32K or 36K non-paged (linear) BIOS, or
- 64K BIOS
- 128K BIOS

Please refer to the *mach64 BIOS Kit (BIO-G01000)* manual for additional information on the differences and trade-offs of the various options.

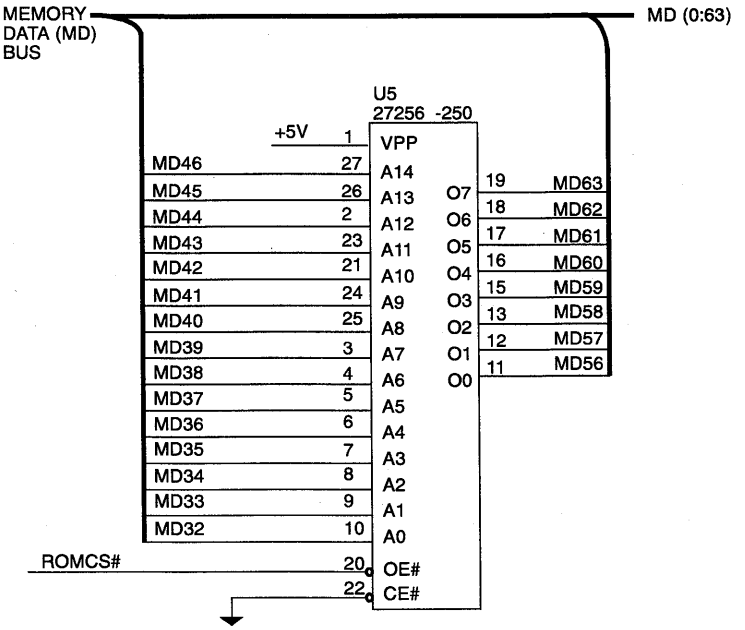

Figure 4-12. EPROM Interface

4.2.10 Flash Memory Interface

Up to 128K of flash memory is supported.

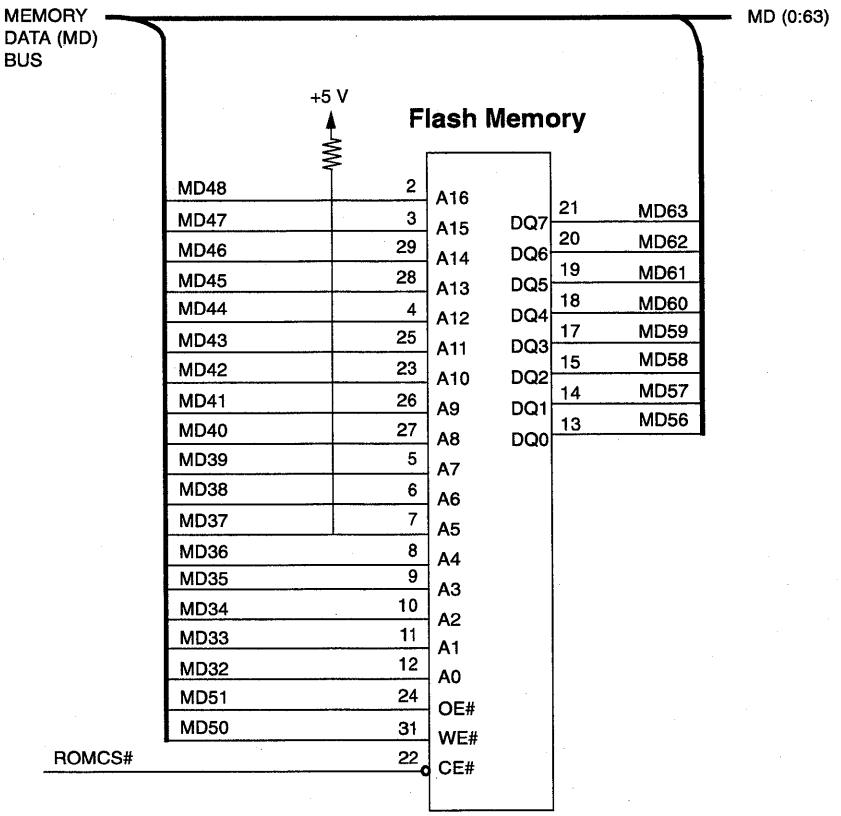

Figure 4-13. Flash Memory Interface

4.3 EEPROM Interface

An optional EEPROM may be added for non-volatile storage of programmable graphics subsystem parameters. It is an alternative to the software-only method of storing timing parameters in a file on a hard drive. However, it is becoming more popular to store parameters in a file for cost reasons. All ATI drivers and utilities support both EEPROM and software-only implementations.

If an EEPROM is present (see *Figure 4-14*), it is re-loaded with user-defined power-on defaults and monitor parameters whenever modifications are made. Users can therefore customize display sizes and positions of various video modes, then store the settings in the EEPROM. When the user selects a customized video mode, the BIOS accesses the EEPROM instead of a monitor timing table of fixed parameters to support that mode. The EEPROM is not supported when the AMC is used for DVS or MPP functions.

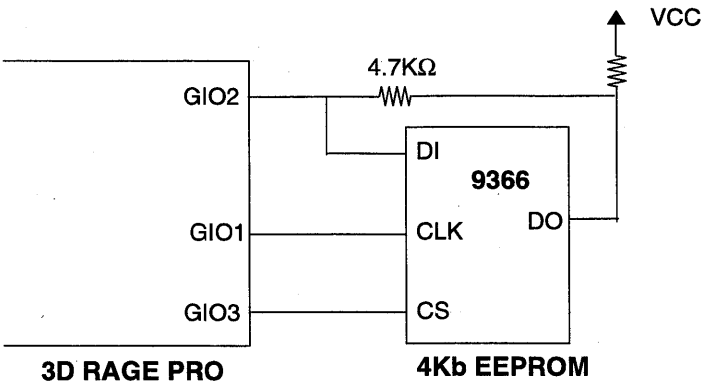

Figure 4-14. EEPROM Interface

The EEPROM used is a 4Kb serial device (P/N 9366) organized as 256 registers of 16 bits. The interface to the EEPROM is straight forward. When the EECS signal from the controller enables access to the EEPROM, data is clocked into the DI port or clocked out from the DO port on the positive edge of the clock signal. The DO/DI, CLK, and CS ports on the EEPROM are connected to the GIO2, GIO1, and GIO3 controller pins respectively.

4.4 General Purpose I/O Control

Within the *3D RAGE PRO* there are two *general purpose* I/O buses used to control optional interfaces — GIO[4:0] and GPIO[F:0]. The GIO is used to support the interfaces for EEPROM, monitor ID, and I^2C bus control. The GPIO is used for the ATI Multimedia Channel interface which is described on the following page (see *Figure 4-15*).

Table 4-2 GIO Bus

GIO	Pin Name	Description
GIO0	GIO0	MONID1-DDC serial data
GIO1	GIO1	EECK
GIO2	GIO2	EEDIO, I^2L-SDA
GIO3	GIO3	EECS
GIO4	GIO4	MONID2-DDC serial clock
GIOC	GIOC	MONID0

Table 4-3 GPIO Bus

GPIO	Pin Name	VFC Mode	DVS Mode	MPP Mode
GPIO0	BLANK#	BLANK#	-	SAD0
GPIO1	GIO6	VFC H SYNC	-	SAD1
GPIO2	GIO5	VFC V SYNC	-	SAD2
GPIO3	GIO7	-	-	SAD3
GPIO4	GIO2	-	SDA	SAD4
GPIO5	GIO9	-	-	SAD5
GPIO6	GIO8	-	-	SAD6
GPIO7	GIO3	-	-	SAD7
GPIO8	EVIDEO	EVIDEO	-	SIOR
GPIO9	ESYNC	ESYNC	-	SIOW
GPIOA	EDCLK	EDCLK	-	SRDY/IRQ
GPIOB	GIO1	-	SCL	-
-	PDATA[7:0]	data[7:0]	YUV[7:0]	-
-	DCLK	DCLK	CLK	-

4.5 ATI Multimedia Channel 2.0 Interface (AMC)

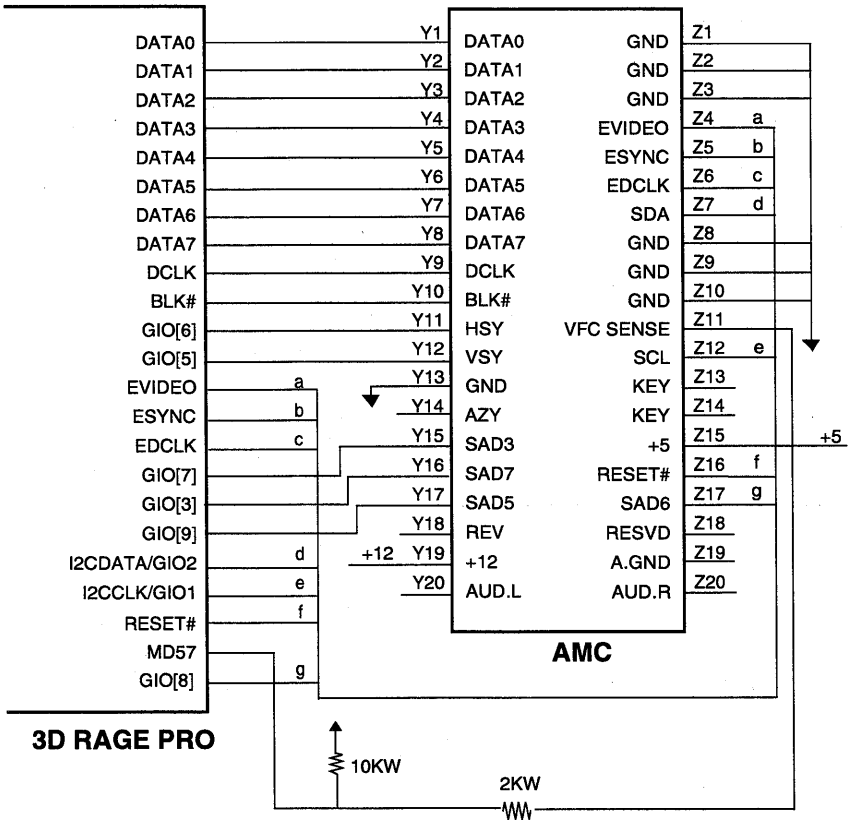

Figure 4-15. ATI Multimedia Channel 2.0

The AMC is a 40-pin connector which can be added to a design based on the *3D RAGE PRO*. The AMC can operate in various modes under different conditions. AMC pins have different functions under different modes, as follows:

VFC Mode — VESA VGA Feature Connector Mode supports various overlay peripherals such as MPEG cards. Output from the VFC may be enabled in all VGA modes as well as accelerated display modes with a display clock below 80MHz.

DVS Mode — Digital Video Stream Mode supports a direct connection to a Brooktree Bt829, Bt827, Bt819, Bt817, or Bt815, and Philips SAA7112 or SAA7111 video decoder. Connection to a Samsung KSO122 or ITT VPC32xx video decoder requires some additional logic.

Depending on the package type, PQFP or BGA, I^2C pins on the AMC connector are driven by different sources.

In PQFP package, the I^2C pins are driven by GIO1 and GIO2 directly, provided there is no TV-out chip on board. If there is TV-out chip, I2C_CLK and I2C_DAT from TV-out chip will be the drivers.

In the BGA package, there are specially dedicated pins — I2CCLK and I2CDATA — to drive the AMC I^2C pins.

MPP Mode — Multimedia Peripheral Port Mode can stream data from the host memory out of this port. Timing and protocol can be programmed to support peripheral chips. By connecting this port to an external NTSC/PAL encoder, the display screen can be modulated to an NTSC/PAL TV signal.

4.6 Analog Output Section

Each of the R, G, B lines on the board (see *Figure 4-16*) is to be loaded with a 75Ω resistor. Diodes can be used to protect the controller from any large transient voltages which may enter from the connector when the monitor is connected.

Bypass capacitors can also be placed on all lines in order to filter the output. The RGB lines may also have inductors (ferrites) placed in series. This may be required in order to comply with FCC Class B requirements for radio frequency emissions. The proper value is determined as a trade-off between filtering the signals for FCC requirements and video signal clarity.

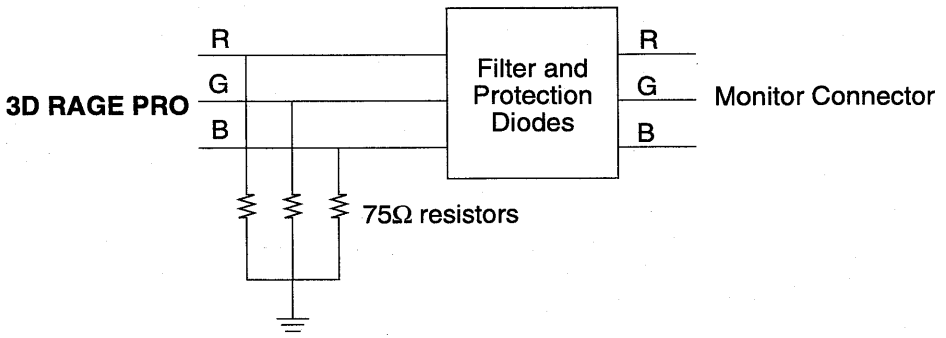

Figure 4-16. Analog Output

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5.1 Strap Resistors Summary

External strap resistors may be used to configure various aspects of the *3D RAGE PRO* graphics subsystem. Logic levels at the strap pins are sensed and latched into registers at the first PCI command. The *3D RAGE PRO* contains internal pull-down resistors on strap pins to provide a default strap value of logic zero. By pulling the strap pin high via an external pull-up resistor, the strap value can be forced to logic one. In some cases, the registers which hold the strapped values are writable by video BIOS. The table below summarizes the strap pins on the controller. It is followed by a section which provides a detailed explanation of each strapping option.

Table 5-1 3D RAGE PRO Strap Resistors

Signal Name	Strap Name	BIOS Configurable	Description
MD63	reserved	n/a	0 = normal operation (default) 1 = reserved
MD62	IDSEL	No	0 = connect IDSEL to AD16 (default) 1 = connect IDSEL to AD17
MD61	ROM_REMAP	No	0 = No ROM Remap (default) 1 = If VGA disabled, remap top 8K to bottom
MD60	reserved	n/a	0 = normal operation (default) 1 = reserved
MD59	ENINT#	No	0 = interrupt enable 1 = interrupt disable (default)
MD58	VGA_DISABLE	No	0 = VGA enable (default) 1 = VGA disable
MD57	VFC_SENSE#	No	0 = VFC mode 1 = AMC mode
MD56	reserved	n/a	0 = normal operation (default) 1 = reserved

Table 5-1 3D RAGE PRO Strap Resistors (Continued)

Signal Name	Strap Name	BIOS Configurable	Description
MD55	TESTEN	No	0 = normal operation (default) 1 = test mode enabled
MD54	reserved	n/a	0 = normal operation (default) 1 = reserved
MD53	PREFETCH_EN	No	0 = disable prefetch 1 = enable prefetch
MD52	reserved	n/a	0 = normal operation (default) 1 = reserved
MD51	ID_DISABLE	No	0 = normal operation (default) 1 = disable controller
MD(50:48)	CFG_MEM_TYPE (2:0)	Yes	(xxxb) = Memory Type (000) = reserved (001) = WRAM (010) = SGRAM (011) = SDRAM (100) = hyper page DRAM or EDO (101) = EDO DRAM (110) = FP DRAM (111) = disable memory access
MD47	MEM_CS_EN	No	0 = tristate CS#0 and CS#1 1 = enable chip select (default)
MD(46:44)	X1CLKSKEW (2:0)	No	AGP X1 clock phase adjustment with respect to X2. (000) = 0.0 nsec (default) (001) = 0.5 nsec (010) = 1.0 nsec (011) = 1.5 nsec (100) = 2.0 nsec (101) = 2.5 nsec (110) = 3.0 nsec (111) = 3.5 nsec

Table 5-1 3D RAGE PRO Strap Resistors (Continued)

Signal Name	Strap Name	BIOS Configurable	Description
MD(43:41)	AGPSKEW (2:0)	No	AGP X1 clock feedback phase adjustment with respect to refclk (cpuclk) (000) = refclk 1 tap earlier than X1 (feedback). Default (001) = refclk 2 taps earlier than X1 (feedback) (010) = refclk 3 taps earlier than X1 (feedback) (011) = agp pll testmode, X2 is used as feedback (100) = feedback (X1) 3 taps earlier than refclk (101) = feedback (X1) 2 taps earlier than refclk (110) = feedback (X1) 1 tap earlier than refclk (111) = feedbacl (X1) and refclk are aligned each tap is worth 5 nsec roughly
MD40	BUS_TYPE	No	0 = normal bus type (default) 1 = alternated bus type
MD(39:38)	AGPVCOGAIN	No	VCO filter gain control (00) = (10) to VCO gain (default), no strap installed (01) = (11) to VCO gain (10) = (00) to VCO gain (11) = (01) to VCO gain
MD(37)	ROMWRTEN	No	0 = EPROM used for video BIOS - PEROM (default) 1 = Flash Memory used for video BIOS
MD(36:32)	reserved - not used	n/a	(xxxxxxb) = don't care
MD(31:29)	SO-DIMM Strap Resistors	No	(xxxb) = determined by SO-DIMM; see SO-DIMM specification
MD(28:24)	reserved - not used	n/a	(xxxxxb) = don't care
MD(23:8)	SUBSYS_VEN_ID(15:0)	Yes	(xxxxh) = PCI subsystem vendor ID
MD(7:0)	SUBSYS_DEV_ID(7:0)	Yes	(xxh) = LSB of PCI subsystem device ID register
PCI33EN	BUS_CLK_SELECT	No	0 = normal bus clock (default). 1 = alternate bus clock

Note: Strap resistors do not need to be installed on X1CLKSKEW and AGPSKEW (**MD(46:44)** and **MD(43:41)** respectively).

5.2 Strap Resistor Description

MD62	IDSEL	No	0 = connect IDSEL to AD16 (default) 1 = connect IDSEL to AD17

This strap has only significance for AGP devices since IDSEL is not a signal in the AGP interface. In an AGP implementation, the initialization device select signaling is provided on AD16 as per the AGP specification. The IDSEL strap allows the alternate AD17 signal to be selected. This alternate IDSEL provides a method of initializing a second graphic controller on the AGP bus in some future application. This strap is not used for the PCI variant of *3D RAGE PRO* since a dedicated IDSEL signal is provided in the PCI bus interface.

MD61	ROM _REMAP	No	0 = No ROM Remap (default) 1 = If VGA disabled, remap top 8K to bottom

If VGA is disabled, this strap permits the remapping of the top 8K of the ROM to the bottom. This strap is only applicable to add-in cards which use a separate video BIOS ROM.

MD59	ENINT#	No	0 = interrupt enable 1 = interrupt disable (default)

The interrupt strap permits enabling or disabling of interrupts. The *3D RAGE PRO* has the capability of generating an interrupt request via the INTA# signal. Strapping MD59 to logic zero places the value 01h in the read-only Interrupt Pin register and enables interrupts. Strapping MD59 to logic one places the value 00h in the interrupt Pin register and disables interrupts. However, disabling the request for an interrupt resource does not prevent the graphics controller form asserting the INTA# signal if it is programmed to do so.

MD58	VGA_DISABLE	No	0 = VGA enable (default) 1 = VGA disable

The VGA disable strap provides a method of disabling the VGA portion of the graphics controller. This feature has possible application in systems containing more than one graphics controller.

MD57	VFC_SENSE#	No	0 = VFC mode 1 = AMC mode

This strap signal is used for detecting the class of peripheral connected to the ATI Multimedia Connector, and configuring the AMC interface for either the AMC or VFC mode of operation. The *3D RAGE PRO* reference design provides an external pull-up resistor on MD57 which forces AMC mode as the default. All VFC peripherals pull MD57 low through a 10K resistor to assert VFC_SENSE#.

MD55	TESTEN	No	0 = normal operation (default) 1 = test mode enabled

This strap is used to place the *3D RAGE PRO* into test mode. Since test mode is only applicable for out-of-circuit testing, the provision for an external strap resistor is not required.

MD53	PREFETCH_EN	No	0 = disable prefetch 1 = enable prefetch

This strap permits the setting of bit 3 in the memory base address register to mark the range as prefetchable (see the description in the PCI specification in Chapter 6). A device can mark a range as prefetchable if there are no side effects on speculative reads, the device returns all bytes on reads regardless of the byte enables, and a host bridge can merge processor writes into this range without causing errors. The *3D RAGE PRO* complies with these requirements.

MD51	ID_ DISABLE	No	0 = normal operation (default) 1 = disable controller

Allows the controller to be deactivated as far as the AGP or PCI bus is concerned. Strapping to disable the controller forces the internal logic for IDSEL to zero which prevents initialization of the device. The device will not respond to any PCI or AGP transactions, and will not drive signals on the AGP or PCI bus when disabled in this way.

MD(50:48)	CFG_MEM_TYPE (2:0)	Yes	(xxxb) = Memory Type (000) = reserved (001) = WRAM (010) = SGRAM (011) = SDRAM (100) = hyper page DRAM or EDO (101) = EDO DRAM (110) = FP DRAM (111) = disable memory access

The memory type straps provide the option of configuring the memory type through external hardware straps. Since most graphics subsystems use a single memory type, the memory type strap resistors are not used. Instead, the video BIOS is designed to load the required value for the memory type in the CFG_MEM TYPE register during system initialization. Video BIOS binary and configuration files are available for the full range of memory types. Note that if external strapping is used, the CFG_MEM_TYPE filled in the CONFIG_STAT0 register contains the inverse of the strapped values.

MD47	MEM_CS_EN	No	0 = tristate CS#0 and CS#1 1 = enable chip select (default)

The MEM_CS_EN strap provides a means of enabling or disabling the output buffers for CS#0 and CS#1. The default setting for MEM_CS_EN is enabled. An external pull-up resistor is required on this strap pin. This strapping enables memory bank selection via the CS#0 and CS#1 signals.

The tristate option is provided for backward compatibility of the *3D RAGE PRO* with designs based on the original *3D RAGE I* component.

MD40	BUS_TYPE	No	0 = normal bus type (default) 1 = alternated bus type

This strapping has meaning for all *3D RAGE PRO* product variants. For devices in a 256 BGA package, the normal bus type is AGP and the alternate bus type is PCI. For devices in a 208 PQFP package, the normal bus type is PCI and the alternate bus type is AGP. For 256 BGA devices, selecting the alternate bus type (i.e., PCI) permits a WRAM-based graphics subsystem to be provided for PCI system. Only the 256 BGA device has a sufficient number of pins to support a WRAM-based frame buffer.

The *3D RAGE PRO G* supports an AGP 66MHz interface in a 208-pin package without sideband addressing. In this configuration, the bus type is strapped as alternate.

MD(39:38)	AGPVCOGAIN	No	VCO filter gain control (00) = (10) to VCO gain (default), no strap installed (01) = (11) to VCO gain (10) = (00) to VCO gain (11) = (01) to VCO gain

These strap pins define the gain of the voltage controlled oscillator (VCO) in the PLL subsystem which generates the internal X1 and X2 AGP clock signals. The gain in the VCO circuit does not necessarily increases with increasing binary values of the strap setting. The default gain strapping of (00b) is the target implementation (i.e., no external resistors). However, the foot print for strap resistor on MD39 and MD38 should be provided on all new *3D RAGE PRO* designs in order to permit future adjustment of the gain control, if required.

MD(37)	ROMWRTEN	No	0 = writable Flash memory not installed 1 = writable Flash Memory installed for video BIOS

The ROMWRTEN strap is installed to indicate that writable Flash memory (PEROM) is being used for the video BIOS.

MD(36:32)	reserved - not used	n/a	(xxxxxb) = don't care

These strap pins are not used. They are reserved for possible future use.

MD(31:29)	SO-DIMM STRAP	No	(xxxb) = determined by SO-DIMM; see SO-DIMM specification

These three bits are mandatory straps on all SO-DIMM modules and indicate the synchronous clock frequency or cycle time of the SO-DIMM. See the SO-DIMM specification for the definition of the strap resistors.

MD(28:24)	reserved - not used	n/a	(xxxxxb) = don't care

These five strap pins are not used. They are reserved for possible future use.

MD(23:8)	SUBSYS_VEN_ID(15:0)	Yes	(xxxxh) = PCI subsystem vendor ID

The subsystem vendor ID is a 16-bit register in PCI configuration space and used to uniquely identify subsystem manufactured by different vendors but with the same PCI or AGP device. The subsystem vendor ID for individual vendors is obtained from the PCI SIG.

The *3D RAGE PRO* supports two methods for loading the subsystem vendor ID register. The first involves writing the register with a customizable value stored in the video BIOS. This is the preferred approach and the one which is generally used. The second method involves strapping the MD(28:8) signals to set the desired vendor ID register value.

MD(7:0)	SUBSYS_DEV_ID(7:0)	Yes	(xxh) = LSB of PCI subsystem device ID register

The subsystem device ID is a 16-bit register in PCI configuration space and is used to identify a vendor's implementation of a particular subsystem. The subsystem device ID is supplied by the vendor. The *3D RAGE PRO* supports two methods for loading the subsystem device ID register. The first involves writing the register with a customizable value stored in the video BIOS. This is the preferred approach and the one which is generally used. The second method involves strapping the MD(7:0) signals for the desired register value. The strapped values on MD(7:0) are mapped to the lower byte of the subsystem device ID register.

PCI33EN	BUS_CLK_SELECT	No	0 = normal bus clock (default) 1 = alternate bus clock

For AGP versions of *3D RAGE PRO*, selecting normal bus clock sets the internal clock to the PLL. Selecting alternate bus clock, sets the internal clock to the external bus clock.

For PCI versions of *3D RAGE PRO*, selecting normal sets the internal clock to the PCI bus clock. Selecting alternate sets the internal clock to the PLL generated clock. The normal setting is the default strapping for both AGP and PCI components. Since the alternate bus clock strapping may be useful during system checkout, initial *3D RAGE PRO* designs should provide the foot print for this strap resistor.

6.1 Table Conventions

Controller pins have different operational characteristics. The assigned codes for each of these pin types are listed below. For electrical characteristics please refer to *Chapter 7 "Timing Specifications"*.

Table 6-1 Conventions

Code	Pin Type / Operational Characteristics
I	Input pin
O	Output pin
I/O	Bi-Directional pin
M	Multifunction pin
Pwr	Power pin
Gnd	Ground pin
A	Analog pins

Pin numbers and signal names are sorted by interface and by pin number on the following pages.

All active-low signal names are identified by the succeeding # character throughout this document, e.g. BLANK#.

The following table shows the support for various buses in either the 208 PQFP package or the 256 BGA package:

Table 6-2 Bus types supported

Bus type	208 PQFP	256 BGA	Description
PCI-33	x	x	PCI bus 33MHz with 5.0V signaling. For standard PCI slot
AGP-66	-	x	66MHz AGP bus with 1X transfer and full sideband signals
AGP-133	-	x	133MHz AGP bus with 2X transfer and full sideband signals

Table 6-3 Clock type determination

Signal Name	Pin Type	Description
PCI33EN	I	Determines the clock type: PCI or AGP clock

6.2 AGP/PCI Bus Interface Implementation

The signals below support the 5V PCI interface.

Table 6-4 AGP/PCI Bus Interface

Signal Name	Pin Type	Description
AD[31:0]	I/O	Multiplexed — System Address or Data bits [31:0]
ADSTB[1:0]	I/O	AD Bus Strobes —- provides tuning for 2x data transfer
C/BE#[3:0]	I/O	Multiplexed — Bus Command or Byte Enable bits 3:0. (BE# is active low)
CPUCLK	I	Bus Clock
DEVSEL#	I/O	Device Select — When driven active "Low", it is indication that the controller has decoded its address. Not used by AGP.
FRAME#	I/O	Frame is driven by the current bus master to indicate the beginning and duration of an access
GNT#	I	Grant — Indicates to the agent that a bus access has been granted
IDSEL	I	Initialization Device Select - Used as a Chip Select during configuration read and write transactions. Used as PIPE# in AGP Bus (always "High").
INTR#	O	Interrupt Request — Level triggered. Active "Low" by default
IRDY#	I/O	Initiator Ready — Indicates the bus master is able to complete the current data phase of the transaction
PAR	I/O	Parity — Even parity used (expand on parity detection)
RBF#	O	Read Buffer Full — Indicates whether the master is ready to accept previously requested low priority read data or not
REQ#	I/O	Request — Indicates to the chip set that there is request for bus master cycle
RESET#	I	Bus Reset
SBA[7:0]	O	Side Band Address Port— Provides additional bus to pass address and command to the target
SBSTB	O	Side Band Strobe — Provides a timing strobe for Sideband Address Port
ST[2:0]	I	Status bus — Provides information from the arbiter to the master on what it may do
STOP#	I/O	Stop — Indicates the current target is requesting the master to stop the current transaction. Not used by AGP
TRDY#	I/O	Target Ready — Indicates the target agent is able to complete the current data phase of the transaction

6.3 Memory Interface

Table 6-5 Memory Interface

Signal Name	Pin Type	Description
CAS#0	M-O	This multifunction pin has the following functions: - Write Strobe WE# for DRAMs (256Kx16x2). Active "Low" - Column Address Strobe CAS#0 for SGRAMs and WRAM
CAS#1	M-O	This multifunction pin has the following functions: - Chip Select CS#3 for SGRAM (128Kx32x2 and 128Kx16x2). Active "Low". - Address Line MA11 for SGRAM (512Kx16x2). - Write Strobe WE#1 for DRAM (128Kx16x2). Active "Low". - Column Address Strobe CAS#1 for WRAM.
CS#[1:0]	M-O	This multifunction pin has the following functions: - Strap PREFETCH/CS(1), 5V tol. Active "Low". - CS(0)for SDRAM, 5V tol. Active "Low". -Column Address Strobe CAS#[3:2] for WRAM.
DSF[2:0]	O	DRAM special function
MA[9:0]	O	Row/Column Address Bus. Multiplexed on the same Pins
MD[63:0]	I/O	Bi-directional memory data bus Also see *Controller Configuration* for power-up setting.
OE#0	M-O	This multifunction pin has the following functions: - Output Enable OE# signal for DRAM and WRAM. - Clock for SGRAM.
OE#1	M-O	Used as: - Write Enable WE# signal for SGRAM. Active 'Low'. - Output Enable OE# for DRAM and WRAM.
RAS#0	O	Used as a Row Address Strobe RAS#. Active "Low"
RAS#1	M-O	This multifunction pin has the following functions: - Chip Select CS#2 for SGRAM (128Kx32x2). Active "Low". - Address Line MA10 for SGRAM (256Kx32x2 and 512Kx16x2). - Row Address Strobe RAS#1 fro DRAM (256Kx16). Active "Low".
WE#[7:0]	M-I/O	This multifunction pin has following functions: - Column Address Strobe CAS#1 for DRAM. - Byte Masking signal for SGRAM and WRAM.
WE#[15:8]	I/O	Used as Byte Masking for WRAM.
WBANK	I/O	Bank select for 16M WRAM. Connects to SE pin of WRAM.

6.4 Monitor Interface

Table 6-6 Monitor Interface

Signal Name	Pin Type	Description
R	A-O	Red analog current output. This can drive doubly terminated 75Ω line
G	A-O	Green analog current output. This can drive doubly terminated 75Ω line
B	A-O	Blue analog current output. This can drive doubly terminated 75Ω line
RSET#	A-I	Current setting resistor for the DAC is connected to this pin.
HSYNC#	O	Horizontal Sync output. Active "Low"
VSYNC#	O	Vertical Sync output. Active "Low"

6.5 External Crystal Interface

Table 6-7 External Crystal Interface

Signal Name	Pin Type	Description
XTALIN[a]	A-I	14.31818 MHz crystal or CMOS oscillator connection
XTALOUT[a]	A-O	14.31818 MHz crystal connection

a. For designs using an external clock source (instead of a crystal): the input XTALIN is CMOS inverter with C_{in} = 0.5pF, and XTALOUT is not connected.

6.6 Optional ATI Multimedia Channel Interface

Table 6-8 AMC Interface

Signal Name	Pin Type	Descriptions		
		DVS mode	VFC mode	MPP mode
PDATA(7:0)		YUV(7:0)	data(7:0)	*
BLANK#	M-I/O	*	Blank Signal	SAD0
DCLK	I/O	CLK	Dot (Pixel) Clock	Dot (Pixel) Clock
EDCLK	M-I	*	Enable Dot (Pixel) Clock	SRDY/IRQ
ESYNC	M-I	*	ESYNC	SIOW
EVIDEO	M-I	*	EVIDEO	SIOR
GIO2	I/O	SDA	*	SAD4
GIO3	I/O	*	*	SAD7
GIO5	M-I/O	*	VFCVSYNC	SAD2
GIO6	M-I/O	*	VFCHSYNC	SAD1
GIO7	I/O	*	*	SAD3
GIO8	I/O	*	*	SAD6
GIO9	I/O	*	*	SAD5
GIO1	I/O	SCL	*	*
GIO0	I/O	*	*	*
GIO4	I/O	*	*	*
GIOC (only with 256 BGA)				

Note: Any extra pins not used (*) in a particular mode can be used as a general purpose I/O pins GPIO.

6.7 I^2C Interface (BGA only)

Table 6-9 I^2C Interface

Signal Name	Pin Type	Description
I2CCLK	I/O	Dedicated I2C clock pin in BGA package
I2CDATA	I/O	Dedicated I2C data pin in BGA package

Note: These pins can also be used as general I/O pins GPIO.

6.8 External DAC Interface

Table 6-10 External DAC Interface

Signal Name	Pin Type	Description
DAC[7:0]	I/O	This Bi-Directional Data Bus is used for external Video Palette
DACRD#	O	This active "Low" Read Strobe is used for the DAC[7:0] Data Bus
DACWR#	O	This active "Low" Write Strobe is used for the DAC[7:0] Data Bus
RS[3:0]	O	These Register Select outputs select the External DAC registers
ODD/EVEN#	O	Indicate the field status to the external DAC
RCLK	I	Reference clock from DAC
OVERSCAN	O	Overscan output. Controls the display of custom screen boarders
DACSEL	O	Internal/external sync DAC select
EXTBLANK	O	Blank for external DAC

6.9 SCAN Testing and Modes

Table 6-11 SCAN Testing

Signal Name	Pin Type	Description
SCANIN	I	Scan chain data input
SCANOUT	O	Scan chain data output
TESTEN	I	Scan test enable

6.10 Optional EEPROM Interface

Table 6-12 EEROM Interface

Signal Name	Pin Type	Description
GIO1	I/O	EEPROM Clock
GIO2	I/O	EEPROM Data I/O
GIO3	O	EEPROM Chip Select

6.11 Optional EPROM Interface

Table 6-13 EPROM Interface

Signal Name	Pin Type	Description
MD [48:32]	I/O	EPROM Address Bus
MD [63:56]	I/O	EPROM Data Bus
ROMCS#	O	ROM Chip Select for AGP-133

6.12 Flash Memory for ROM

Table 6-14 Flash Memory Interface

Signal Name	Pin Type	Description
MD[48:32]	I/O	Flash Memory Address Bus
ROMCS#	O	Chip Enable
MD(51)	I/O	Output Enable
MD(50)	I/O	Write Enable
MD[63:56]	I/O	Flash Memory Data Bus

6.13 Monitor ID for DDC Support

Table 6-15 Monitor ID

Signal Name	Pin Type	Description
GIO0	I/O	DDC Serial Data
GIO4	I/O	DDC Serial Clock
GIOC	I/O	MONID for Apple monitor

6.14 Power and Ground Pins

Table 6-16 Power and Ground Pins

Signal Name	Pin Type	Description
AVDD	PWR	DAC Analog Power, 3.3V
AVSS	GND	DAC Analog Ground
PVDD	PWR	PLL Power, 3.3V
PVSS	GND	PLL Ground
VDDC for 208 PQFP	PWR	3.3V Power (Core)
VDDR for 208 PQFP	PWR	3.3V Power (I/O ring)
VDD for 256 BGA	PWR	3.3V Power (Core and I/O)
VPP	PWR	5.0V Power (PCI Bus) **or** 3.3V Power (AGP Bus)
VSS	GND	Ground

6.15 3D RAGE PRO Pin Listings (256-pin BGA)

Table 6-17 256 BGA Pinout by Ball Reference

Ball Ref.	Signal Name	Ball Ref.	Signal Name	Ball Ref.	Signal Name	Ball Ref.	Signal Name
A1	I2CDATA	B14	AD14	D7	CS#0	G4	MD0
A2	OE#1	B15	PAR	D8	VSS	G17	AD30
A3	OE#0	B16	SBA5	D9	AD4	G18	AD31
A4	MA7	B17	IRDY#	D10	VDD	G19	REQ#
A5	MA3	B18	AD19	D11	ADSTB0	G20	GNT#
A6	MA0	B19	AD20	D12	VSS	H1	MD5
A7	TESTEN	B20	AD23	D13	AD12	H2	DAC3
A8	AD0	C1	WE#3	D14	AD15	H3	GIOC
A9	AD1	C2	WE#5	D15	DEVSEL#	H4	MD4
A10	AD5	C3	WE#7	D16	VDD	H17	VDD
A11	AD7	C4	MA9	D17	VSS	H18	INTR#
A12	N/C	C5	MA5	D18	AD22	H19	ST2
A13	AD10	C6	MA2	D19	AD25	H20	SBSTB
A14	AD13	C7	CS#1	D20	AD26	J1	MD6
A15	C/BE#1	C8	VPP	E1	DSF0	J2	MD8
A16	TRDY#	C9	AD3	E2	DSF1	J3	MD7
A17	AD16	C10	VPP	E3	DSF2	J4	VDD
A18	AD18	C11	C/BE#0	E4	VDD	J9	VSS
A19	AD17	C12	VPP	E17	N/C	J10	VSS
A20	AD21	C13	AD9	E18	AD24	J11	VSS
B1	WE#6	C14	VPP	E19	AD28	J12	VSS
B2	I2CCLK	C15	STOP#	E20	AD29	J17	ST0
B3	RAS#1	C16	FRAME#	F1	WE#0	J18	ST1
B4	MA8	C17	C/BE#2	F2	DAC2	J19	RBF#
B5	MA4	C18	ADSTB1	F3	DAC1	J20	SBA4
B6	MA1	C19	IDSEL	F4	DAC0	K1	DAC4
B7	PCI33EN	C20	C/BE#3	F17	VPP	K2	GIO9
B8	SBA7	D1	WE#1	F18	AD27	K3	MD10
B9	AD2	D2	WE#2	F19	CPUCLK	K4	MD9
B10	AD6	D3	WE#4	F20	RESET#	K9	VSS
B11	SBA6	D4	RAS#0	G1	MD3	K10	VSS
B12	AD8	D5	MA6	G2	MD2	K11	VSS
B13	AD11	D6	VDD	G3	MD1	K12	VSS

Table 6-17 256 BGA Pinout by Ball Reference (Continued)

Ball Ref.	Signal Name	Ball Ref.	Signal Name	Ball Ref.	Signal Name	Ball Ref.	Signal Name
K17	VDD	N20	PVDD	U11	VDD	W6	RCLK
K18	N/C	P1	DAC5	U12	MD58	W7	MD41
K19	SBA3	P2	MD19	U13	VDD	W8	MD45
K20	SBA2	P3	MD20	U14	MD63	W9	MD48
L1	CAS#1	P4	MD21	U15	VSS	W10	RS3
L2	CAS#0	P17	VPP	U16	DATA3	W11	MD53
L3	MD11	P18	GIO7	U17	WE#13	W12	MD56
L4	VDD	P19	AVSS	U18	EDCLK	W13	MD60
L9	VSS	P20	RSET	U19	ESYNC	W14	MD61
L10	VSS	R1	MD22	U20	GIO8	W15	EXTBLANK
L11	VSS	R2	MD23	V1	SCANIN	W16	DATA5
L12	VSS	R3	MD24	V2	SCANOUT	W17	DATA1
L17	SBA1	R4	VDD	V3	WE#9	W18	WE#11
L18	SBA0	R17	ROMCS#	V4	MD33	W19	XTALOUT
L19	EVIDEO	R18	GIO3	V5	MD37	W20	GIO1
L20	HSYNC#	R19	GIO4	V6	ODD/EVEN#	Y1	DACRD#
M1	MD12	R20	AVSS	V7	MD40	Y2	MD30
M2	MD13	T1	DAC6	V8	MD44	Y3	MD32
M3	MD14	T2	MD25	V9	MD47	Y4	MD36
M4	MD15	T3	MD26	V10	MD51	Y5	DACSEL
M9	VSS	T4	MD27	V11	MD54	Y6	MD39
M10	VSS	T17	WE#15	V12	MD57	Y7	MD42
M11	VSS	T18	DCLK	V13	RS1	Y8	MD46
M12	VSS	T19	BLANK#	V14	MD62	Y9	MD49
M17	VDD	T20	GIO2	V15	DATA7	Y10	RS2
M18	PVSS	U1	MD28	V16	DATA4	Y11	MD52
M19	AVDD	U2	MD29	V17	DATA0	Y12	MD55
M20	VSYNC#	U3	DAC7	V18	WE#14	Y13	MD59
N1	MD16	U4	VSS	V19	GIO0	Y14	RS0
N2	MD17	U5	MD34	V20	OVERSCAN	Y15	WBANK
N3	GIO6	U6	GIO5	W1	WE#8	Y16	DATA6
N4	MD18	U7	VDD	W2	DACWR#	Y17	DATA2
N17	R	U8	MD43	W3	MD31	Y18	WE#10
N18	G	U9	VDD	W4	MD35	Y19	WE#12
N19	B	U10	MD50	W5	MD38	Y20	XTALIN

Table 6-18 256 BGA Pinout by Signal name

Signal Name	Ball Ref.	Signal Name	Ball Ref.	Signal Name	Ball Ref.
AD0	A8	AVDD	M19	DSF0	E1
AD1	A9	AVSS	P19, R20	DSF1	E2
AD2	B9	B	N19	DSF2	E3
AD3	C9	BLANK#	T19	EDCLK	U18
AD4	D9	CAS#0	L2	ESYNC	U19
AD5	A10	CAS#1	L1	EVIDEO	L19
AD6	B10	C/BE#0	C11	EXTBLANK	W15
AD7	A11	C/BE#1	A15	FRAME#	C16
AD8	B12	C/BE#2	C17	HSYNC#	L20
AD9	C13	C/BE#3	C20	I2CCLK	B2
AD10	A13	CPUCLK	F19	I2CDATA	A1
AD11	B13	CS#0	D7	IDSEL	C19
AD12	D13	CS#1	C7	INTR#	H18
AD13	A14	DAC0	F4	IRDY#	B17
AD14	B14	DAC1	F3	G	N18
AD15	D14	DAC2	F2	GIOC	H3
AD16	A17	DAC3	H2	GIO0	V19
AD17	A19	DAC4	K1	GIO1	W20
AD18	A18	DAC5	P1	GIO2	T20
AD19	B18	DAC6	T1	GIO3	R18
AD20	B19	DAC7	U3	GIO4	R19
AD21	A20	DACRD#	Y1	GIO5	U6
AD22	D18	DACSEL	Y5	GIO6	N3
AD23	B20	DACWR#	W2	GIO7	P18
AD24	E18	DATA0	V17	GIO8	U20
AD25	D19	DATA1	W17	GIO9	K2
AD26	D20	DATA2	Y17	GNT#	G20
AD27	F18	DATA3	U16	MA0	A6
AD28	E19	DATA4	V16	MA1	B6
AD29	E20	DATA5	W16	MA2	C6
AD30	G17	DATA6	Y16	MA3	A5
AD31	G18	DATA7	V15	MA4	B5
ADSTB0	D11	DCLK	T18	MA5	C5
ADSTB1	C18	DEVSEL#	D15	MA6	D5

Table 6-18 256 BGA Pinout by Signal name (Continued)

Signal Name	Ball Ref.	Signal Name	Ball Ref.	Signal Name	Ball Ref.
MA7	A4	MD31	W3	ODD/EVEN#	V6
MA8	B4	MD32	Y3	OE#0	A3
MA9	C4	MD33	V4	OE#1	A2
MD0	G4	MD34	U5	OVERSCAN	V20
MD1	G3	MD35	W4	PAR	B15
MD2	G2	MD36	Y4	PCI33EN	B7
MD3	G1	MD37	V5	PVDD	N20
MD4	H4	MD38	W5	PVSS	M18
MD5	H1	MD39	Y6	R	N17
MD6	J1	MD40	V7	RAS#0	D4
MD7	J3	MD41	W7	RAS#1	B3
MD8	J2	MD42	Y7	RBF#	J19
MD9	K4	MD43	U8	RCLK	W6
MD10	K3	MD44	V8	REQ#	G19
MD11	L3	MD45	W8	RESET#	F20
MD12	M1	MD46	Y8	ROMCS#	R17
MD13	M2	MD47	V9	RS0	Y14
MD14	M3	MD48	W9	RS1	V13
MD15	M4	MD49	Y9	RS2	Y10
MD16	N1	MD50	U10	RS3	W10
MD17	N2	MD51	V10	RSET	P20
MD18	N4	MD52	Y11	SBA0	L18
MD19	P2	MD53	W11	SBA1	L17
MD20	P3	MD54	V11	SBA2	K20
MD21	P4	MD55	Y12	SBA3	K19
MD22	R1	MD56	W12	SBA4	J20
MD23	R2	MD57	V12	SBA5	B16
MD24	R3	MD58	U12	SBA6	B11
MD25	T2	MD59	Y13	SBA7	B8
MD26	T3	MD60	W13	SBSTB	H20
MD27	T4	MD61	W14	SCANIN	V1
MD28	U1	MD62	V14	SCANOUT	V2
MD29	U2	MD63	U14	STOP#	C15
MD30	Y2	N/C	A12, E17, K18	ST0	J17

Table 6-18 256 BGA Pinout by Signal name (Continued)

Signal Name	Ball Ref.	Signal Name	Ball Ref.	Signal Name	Ball Ref.
ST1	J18	VSS	K10, K11, K12, L9,	WE#6	B1
ST2	H19		L10, L11, L12, M9,	WE#7	C3
TESTEN	A7		M10, M11, M12, U4,	WE#8	W1
TRDY#	A16		U15	WE#9	V3
VDDC	D16, K17, L4, U11	VSYNC#	M20	WE#10	Y18
VDDR	D6, D10, E4, H17,	WBANK	Y15	WE#11	W18
	J4, M17, R4, U7,	WE#0	F1	WE#12	Y19
	U9, U13	WE#1	D1	WE#13	U17
VPP	C8, C10, C12	WE#2	D2	WE#14	V18
	C14, F17, P17	WE#3	C1	WE#15	T17
VSS	D8, D12, D17, J9,	WE#4	D3	XTALIN	Y20
	J10, J11, J12, K9,	WE#5	C2	XTALOUT	W19

6.15.1 3D RAGE PRO Diagram (256-pin BGA Pack)

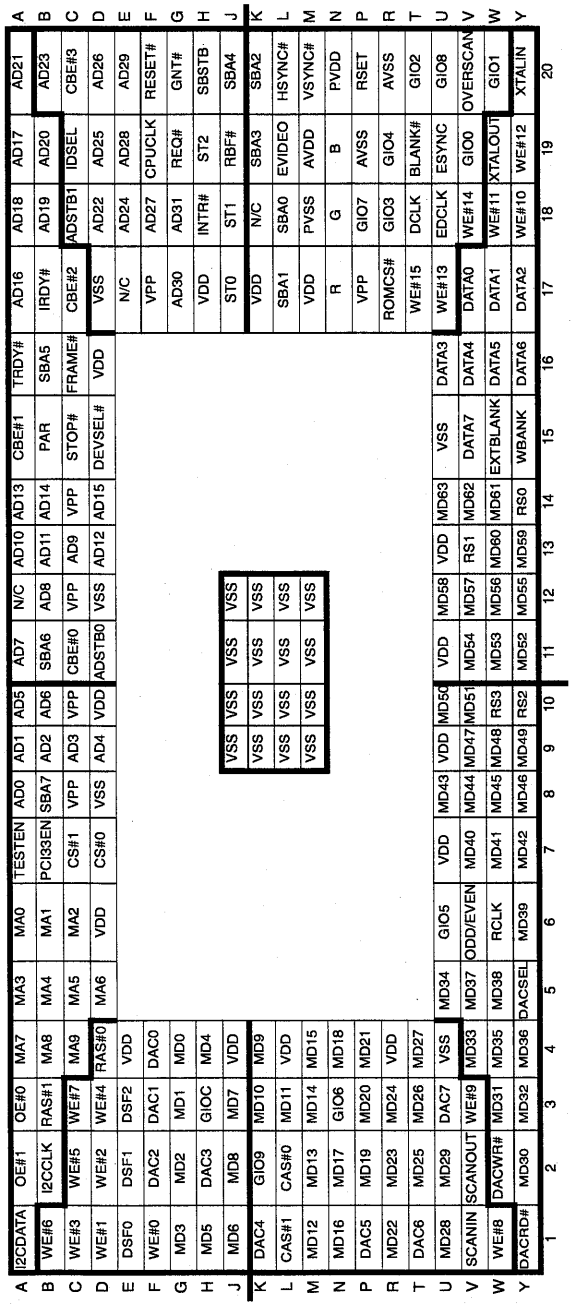


Figure 6-1. 27mm x 27mm BGA Package with 16 Ground Balls at the centre

6.16 3D RAGE PRO Pin Listings (208-pin PQFP)

Table 6-19 208 PQFP Pinout by Pin Number

Pin No.	Signal name	Pin No	Signal Name
1	VSS	2	VSS
3	RAS#0	4	WE#7
5	WE#6	6	WE#5
7	WE#4	8	WE#3
9	WE#2	10	VDD
11	WE#1	12	VSS
13	WE#0	14	MD0
15	MD1	16	MD2
17	MD3	18	MD4
19	MD5	20	MD6
21	MD7	22	MD8
23	MD9	24	MD10
25	GIO9	26	VSS
27	VDD	28	CAS#1
29	CAS#0	30	MD11
31	MD12	32	MD13
33	MD14	34	MD15
35	MD16	36	MD17
37	GIO6	38	MD18
39	VSS	40	MD19
41	MD20	42	MD21
43	MD22	44	MD23
45	MD24	46	MD25
47	MD26	48	MD27
49	MD28	50	MD29
51	VSS	52	VSS
53	VDD	54	MD30
55	MD31	56	MD32
57	MD33	58	MD34
59	MD35	60	MD36
61	MD37	62	GIO5
63	MD38	64	VSS
65	MD39	66	MD40
67	MD41	68	MD42

Table 6-19 208 PQFP Pinout by Pin Number (Continued)

Pin No.	Signal name	Pin No	Signal Name
69	MD43	70	MD44)
71	MD45	72	MD46
73	MD47	74	MD48
75	MD49	76	MD50
77	MD51	78	VDD
79	VSS	80	MD52
81	MD53	82	MD54
83	MD55	84	MD56
85	MD57	86	MD58
87	MD59	88	MD60
89	VDD	90	MD61
91	MD62	92	MD63
93	PIXEL7	94	PIXEL6
95	PIXEL5	96	PIXEL4
97	PIXEL3	98	PIXEL2
99	PIXEL1	100	PIXEL0
101	VSS	102	XTALIN
103	XTALOUT	104	VDDR
105	VSS	106	VSS
107	EDCLK	108	GIO0
109	GIO1	110	CS#1
111	GIO8	112	CS#0
113	ROMCS#	114	DSF (for SGRAM)
115	GIO4	116	GIO2
117	GIO7	118	AVSS
119	AVSS	120	R
121	G	122	B
123	RSET	124	PVDD
125	PVSS	126	AVDD
127	VDDR	128	VSYNC#
129	HSYNC#	130	VDDC
131	VSS	132	EVIDEO
133	RBF#	134	DCLK
135	BLANK#	136	GIO3
137	GNT#	138	REQ#

Table 6-19 208 PQFP Pinout by Pin Number (Continued)

Pin No.	Signal name	Pin No	Signal Name
139	VPP	140	INTR#
141	RESET#	142	CPUCLK
143	AD31	144	AD30
145	AD29	146	AD28
147	AD27	148	AD26
149	AD25	150	AD24
151	C/BE#3	152	IDSEL
153	AD23	154	AD22
155	VSS	156	VSS
157	VDDC	158	AD21
159	AD20	160	AD19
161	AD18	162	AD17
163	AD16	164	C/BE#2
165	FRAME#	166	IRDY#
167	TRDY#	168	VSS
169	DEVSEL#	170	VPP
171	STOP#	172	PAR
173	C/BE#1	174	AD15
175	AD14	176	AD13
177	AD12	178	AD11
179	AD10	180	AD9
181	AD8	182	VSS
183	VPP	184	C/BE#0
185	AD7	186	AD6
187	AD5	188	AD4
189	AD3	190	AD2
191	AD1	192	AD0
193	MA0	194	MA1
195	VDDC	196	MA2
197	VSSC	198	MA3
199	MA4	200	MA5
201	MA6	202	MA7
203	MA8	204	MA9
205	OE#0	206	RAS#1
207	OE#1	208	VDDR

Table 6-20 208 PQFP Pinout by Signal Name

Signal Name	Pin No.	Signal Name	Pin No.
AD0	192	AD1	191
AD2	190	AD3	198
AD4	188	AD5	187
AD6	186	AD7	185
AD8	181	AD9	180
AD10	179	AD11	178
AD12	177	AD13	176
AD14	175	AD15	174
AD16	163	AD17	162
AD18	161	AD19	160
AD20	159	AD21	158
AD22	154	AD23	153
AD24	150	AD25	149
AD26	148	AD27	147
AD28	146	AD29	145
AD30	144	AD31	143
AVDD	126	AVSS	118
AVSS	119	B	122
BLANK#	135	C/BE#0	184
C/BE#1	173	C/BE#2	164
C/BE#3	151	CAS#/WE#	29
CAS#/WE#	128	CPUCLK	142
CS#0	112	CS#1	110
DCLK	134	DEVSEL#	169
DSF (for SGRAM)	114	EDCLK	107
EVIDEO	132	FRAME#	165
G	121	GIO0	108
GIO1	109	GIO2	116
GIO3	136	GIO4	115
GIO5	62	GIO6	37
GIO7	117	GIO8	111
GIO9	25	GNT#	137
HSYNC#	129	IDSEL	152
INTR#	140	IRDY#	166

Table 6-20 208 PQFP Pinout by Signal Name (Continued)

Signal Name	Pin No.	Signal Name	Pin No.
MA0	193	MA1	194
MA2	196	MA3	198
MA4	199	MA5	200
MA6	201	MA7	202
MA8	203	MA9	204
MD0	14	MD1	15
MD2	16	MD3	17
MD4	18	MD5	19
MD6	20	MD7	21
MD8	22	MD9	23
MD10	24	MD11	30
MD12	31	MD13	32
MD14	33	MD15	34
MD16	35	MD17	36
MD18	38	MD19	40
MD20	41	MD21	42
MD22	43	MD23	44
MD24	45	MD25	46
MD26	47	MD27	48
MD28	49	MD29	50
MD30	54	MD31	55
MD32	56	MD33	57
MD34	58	MD35	59
MD36	60	MD37	61
MD38	63	MD39	65
MD40	66	MD41	67
MD42	68	MD43	69
MD44	70	MD45	71
MD46	72	MD47	73
MD48	74	MD49	75
MD50	76	MD51	77
MD52	80	MD53	81
MD54	82	MD55	83
MD56	84	MD57	85
MD58	86	MD59	87

Table 6-20 208 PQFP Pinout by Signal Name (Continued)

Signal Name	Pin No.	Signal Name	Pin No.
MD60	88	MD61	89
MD62	91	MD63	92
OE#0	205	OE#1	207
PAR	172	PIXEL0	100
PIXEL1	99	PIXEL2	98
PIXEL3	97	PIXEL4	96
PIXEL5	95	PIXEL6	94
PIXEL7	93	PVDD	124
PVSS	125	R	120
RAS#0	3	RAS#1	206
RBF#	133	RESET#	141
ROMCS#	113	REQ#	138
RSET	123	STOP#	171
TRDY#	167	VDDC	27
VDDC	78	VDDC	130
VDDC	157	VDDC	195
VDDR	10	VDDR	53
VDDR	89	VDDR	104
VDDR	127	VDDR	208
VPP	139	VPP	170
VPP	183	VSS	1
VSS	2	VSS	12
VSS	26	VSS	39
VSS	51	VSS	52
VSS	64	VSS	79
VSS	101	VSS	105
VSS	106	VSS	131
VSS	155	VSS	156
VSS	168	VSS	182
VSS	197	VSYNC#	128
WE#0 (CAS#, DQM#)	13	WE#1 (CAS#, DQM#)	11
WE#2 (CAS#, DQM#)	9	WE#3 (CAS#, DQM#)	8
WE#4 (CAS#, DQM#)	7	WE#5 (CAS#, DQM#)	6
WE#6 (CAS#, DQM#)	5	WE#7 (CAS#, DQM#)	4
XTALIN	102	XTALOUT	103

6.16.1 3D RAGE PRO PQFP Diagram

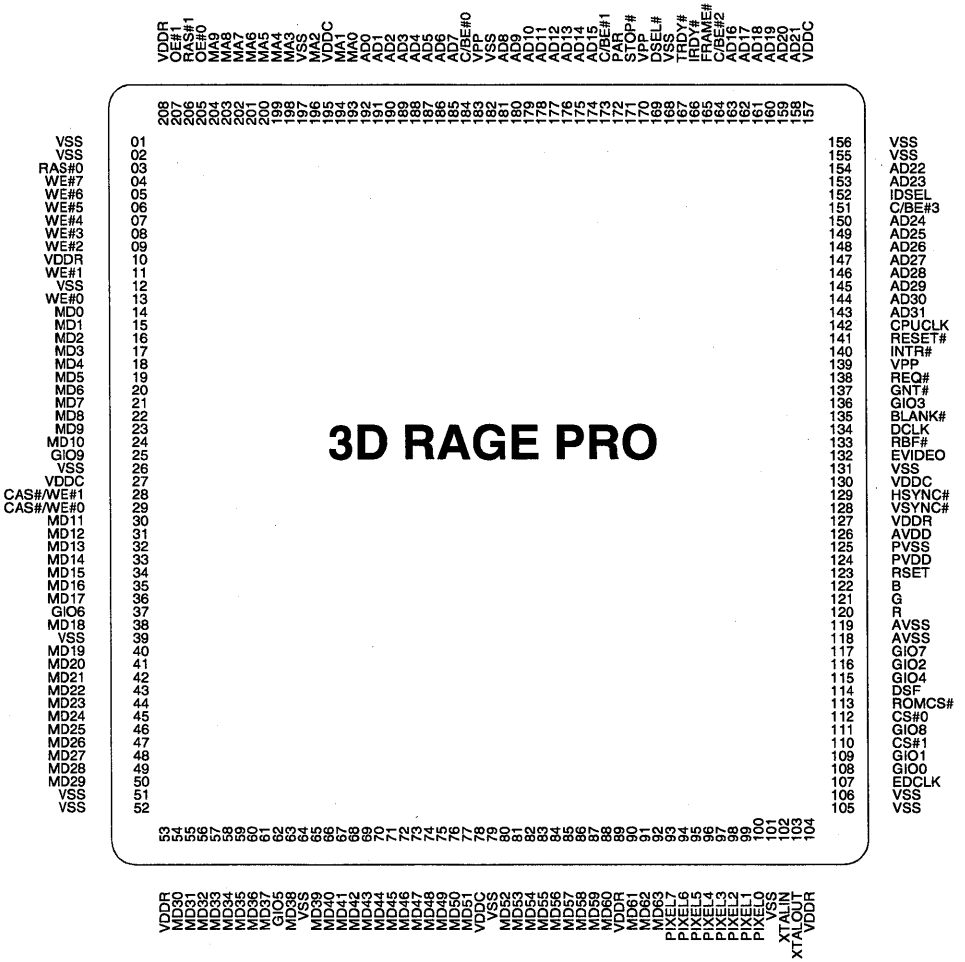


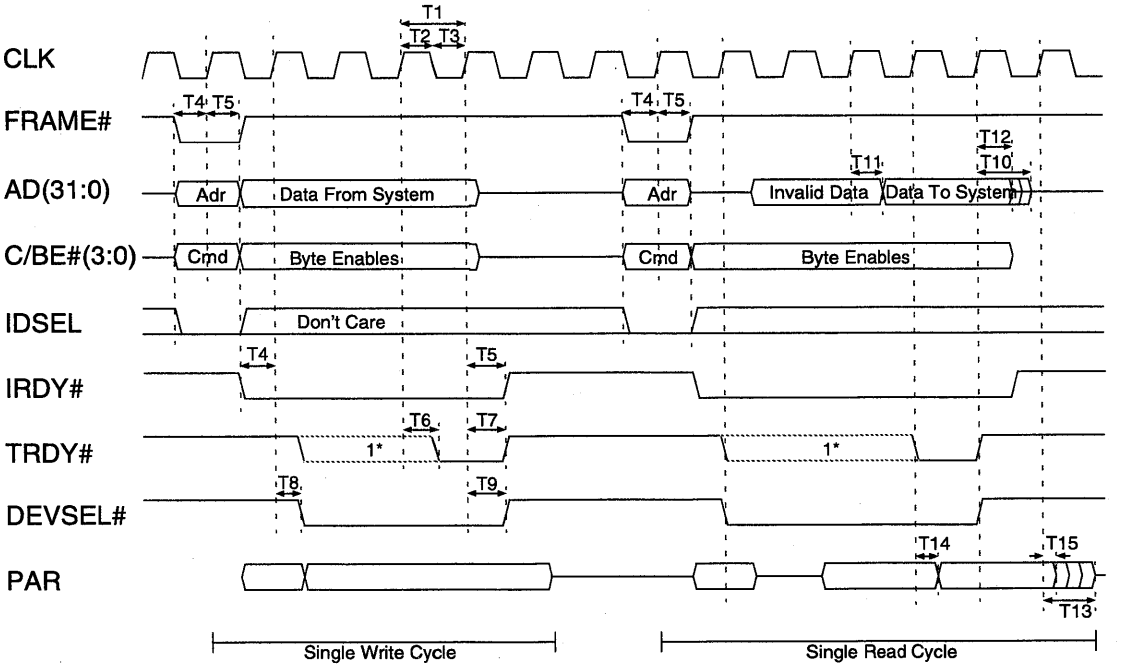
Figure 6-2. 3D RAGE PRO PQFP Pinout

7.1 3D RAGE PRO Bus Timing

Timing specifications for PCI and AGP bus operations are given by:

- Single Read/Write Cycle Timing, see *Figure 7-1.*
- Disconnect On Burst Cycle, see *Figure 7-2.*
- Burst Access Timing, see *Figure 7-3.*
- PCI Bus Master Operation, see *Figure 7-4.*
- AGP AC Timing, see *Figure 7-5* and *Figure 7-6.*

7.1.1 Single Read/Write Cycle Timing



1* The minimum number of clocks from FRAME# active to TRDY# active is programmable.

Figure 7-1. Single Read/Write Cycle Timing - PCI Bus

7.1.2 Disconnect On Burst Cycle - PCI Bus

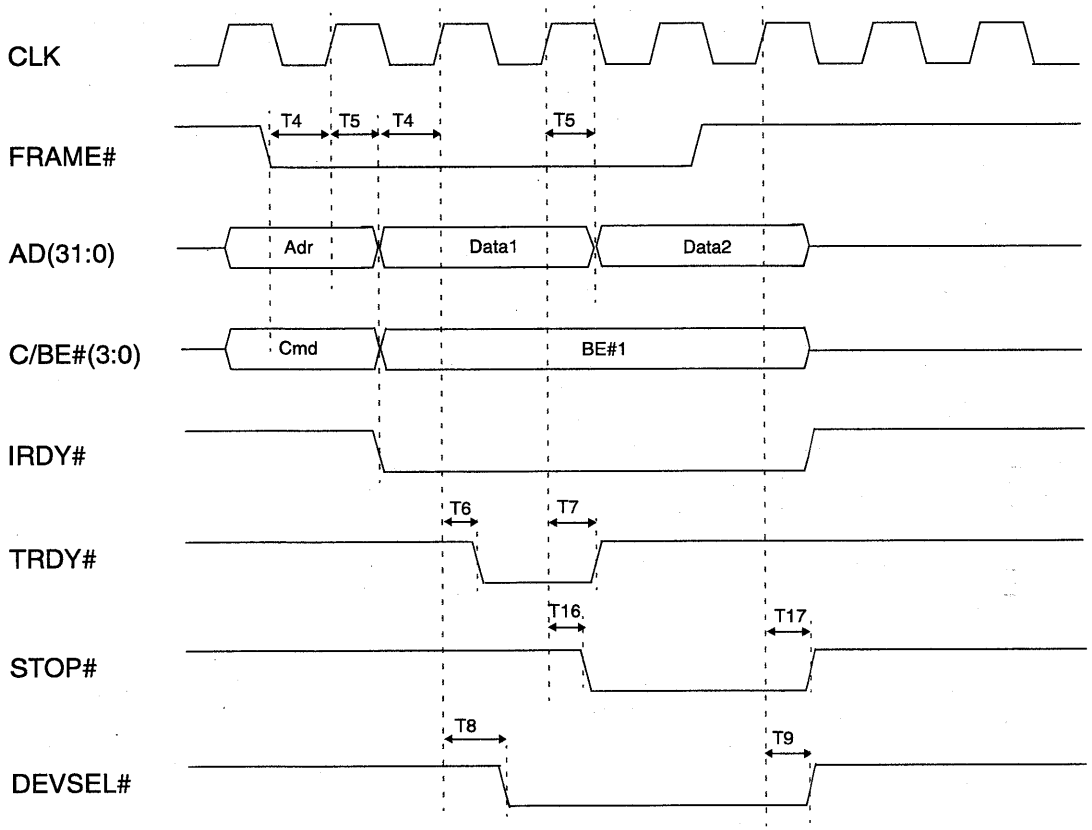


Figure 7-2. Disconnect On Burst Cycle - PCI Bus

7.1.3 Burst Access Timing - PCI

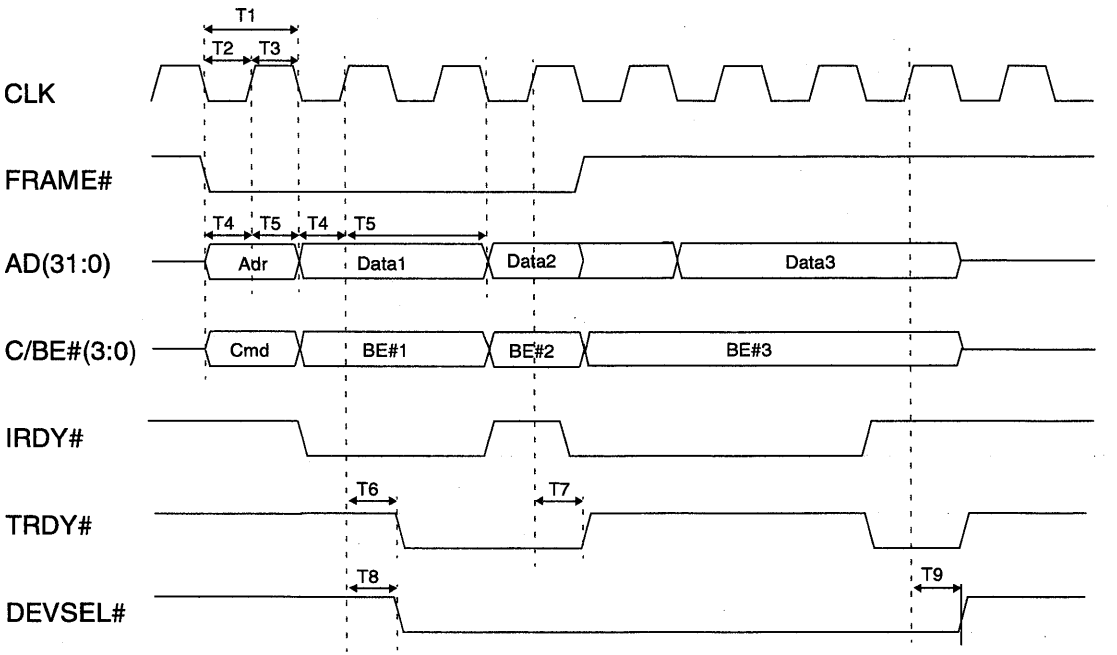


Figure 7-3. Burst Access Timing - PCI Bus

7.1.4 PCI Bus Master Operation

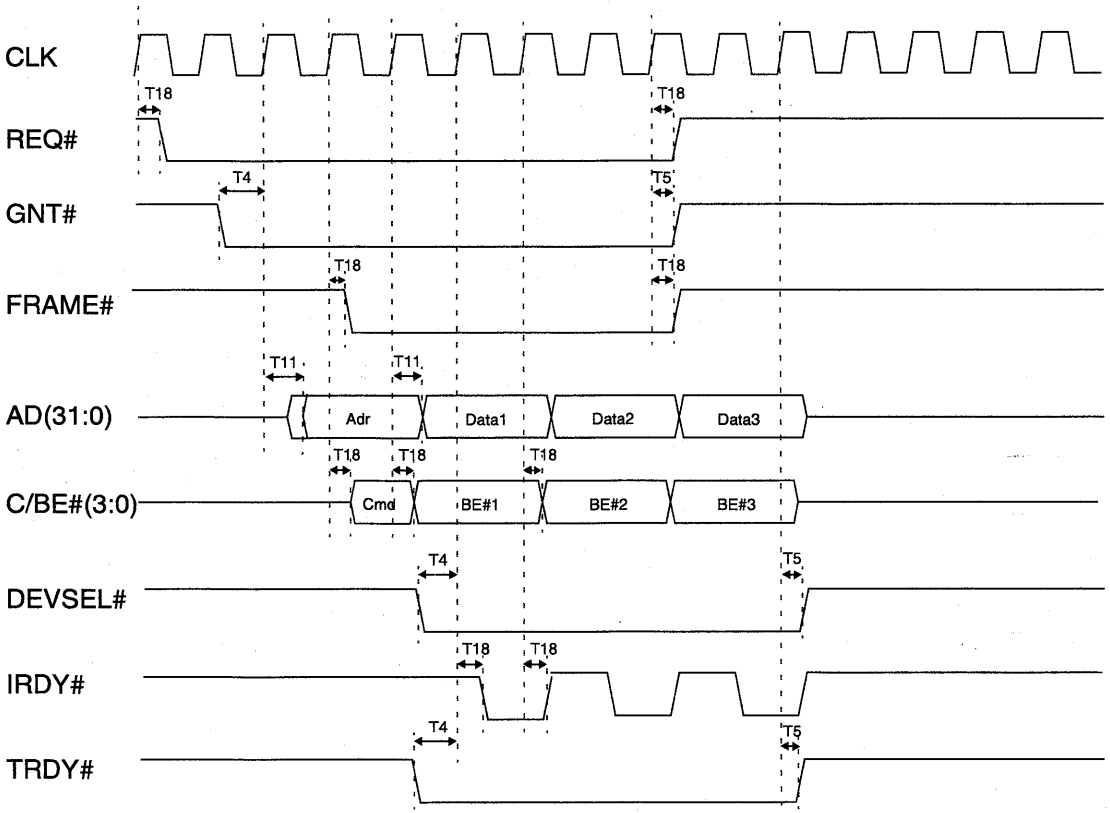


Figure 7-4. PCI Bus Master Operation

Table 7-1 PCI Bus Interface Timing Values

Symbol	Description	Min.(ns)	Max.(ns)
T1	Bus Clock Period	30	-
T2	Bus Clock High Time	12	-
T3	Bus Clock Low Time	12	-
T4	Bus Input Signal Setup to CLK[a]	7	-
T5	Bus Input Signal Hold from CLK[a]	0	-
T6	CLK to TRDY# active	2	11
T7	CLK to TRDY# inactive	2	11
T8	CLK to DEVSEL# active	2	11
T9	CLK to DEVSEL# inactive	2	11
T10	CLK to data output tri-state	2	20
T11	CLK to data output valid delay (data stepping buffer)	2	20
T12	CLK to data output invalid delay	2	-
T13	CLK to PAR tri-state	2	20
T14	CLK to PAR valid delay (data stepping buffer)	2	20
T15	CLK to PAR invalid delay	2	-
T16	CLK to STOP# active delay	2	11
T17	CLK to STOP# inactive delay	2	11
T18	CLK to signal valid delay	2	11

a. Bus input signals include FRAME#, AD(31-0), IDSEL, IRDY#, TRDY#, GNT#, DEVSEL#.

7.1.5 AGP Timing

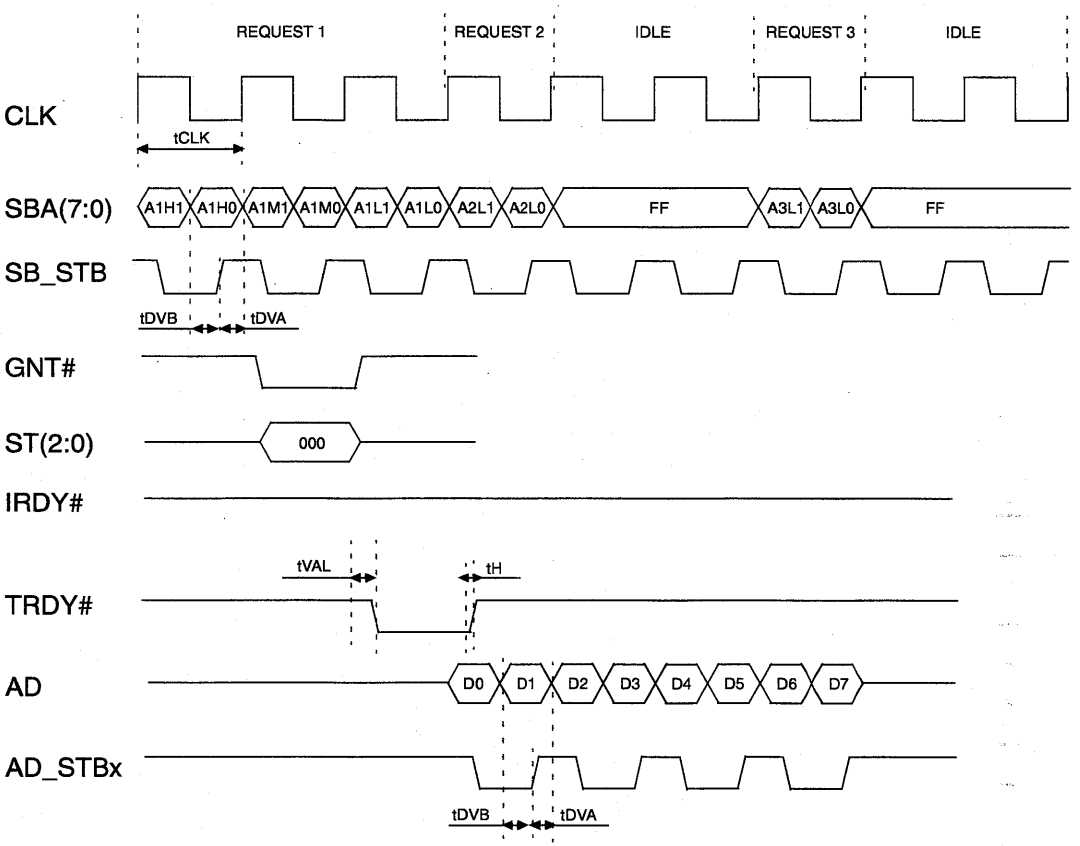


Figure 7-5. AGP 2X Read Request with Return Data (4Qw)

Table 7-2 AGP 2X Timing Parameters

Symbol	Description	Min.(ns)	Max.(ns)
tCLK	Clock	-	15
tDVB	Data valid before	1.7	
tDVA	Data valid after	1.7	-
tVAL	CLK to control signal and Data valid delay	1	5.5
tH	Control signals hold time to CLK	0	-

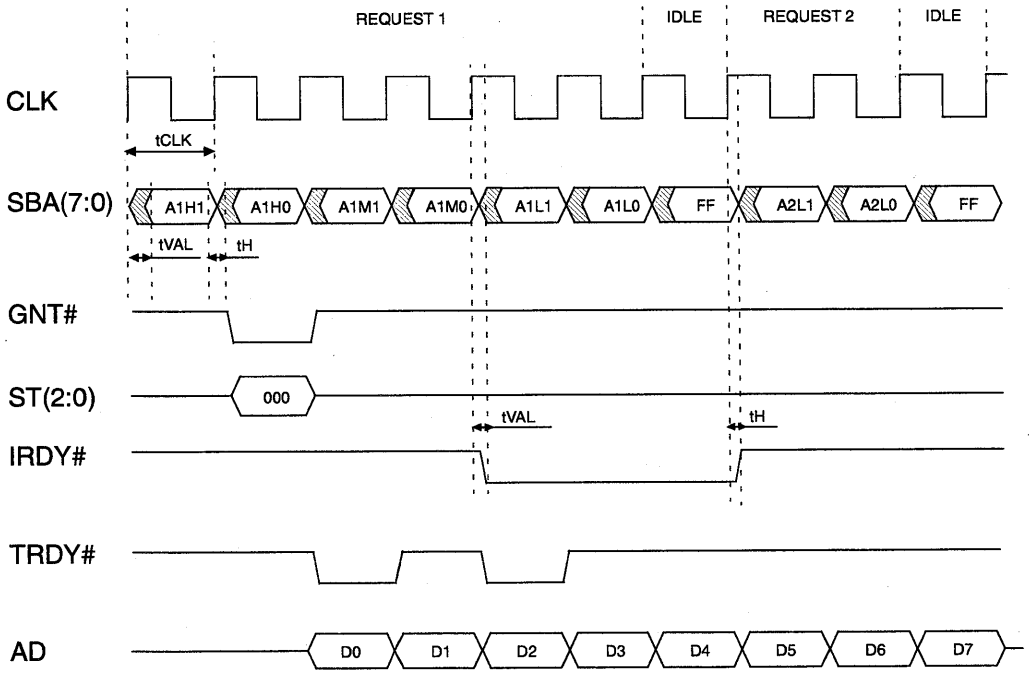


Figure 7-6. AGP 1X Read Request with Return Data (4Qw)

Table 7-3 AGP 1X Timing Parameters

Symbol	Description	Min.(ns)	Max.(ns)
tVAL	CLK to control signal and Data valid delay	1	5.5
tH	Control signals hold time to CLK	0	-

7.2 Memory Timing

Timing Specifications for DRAM / EDO DRAM, SDRAM / SGRAM, and WRAM memory operations are given by:

- DRAM / EDO DRAM Cycle Timing, see *Figure 7-7.*
- Hyperpage EDO DRAM Cycle Timing, see *Figure 7-8.*
- WRAM Cycle Timing, see *Figure 7-9.*
- Refresh Cycle Timing, see *Figure 7-10.*
- SDRAM/SGRAM Cycle Timing, see *Figure 7-11.*

7.2.1 DRAM/EDO DRAM Cycle Timing

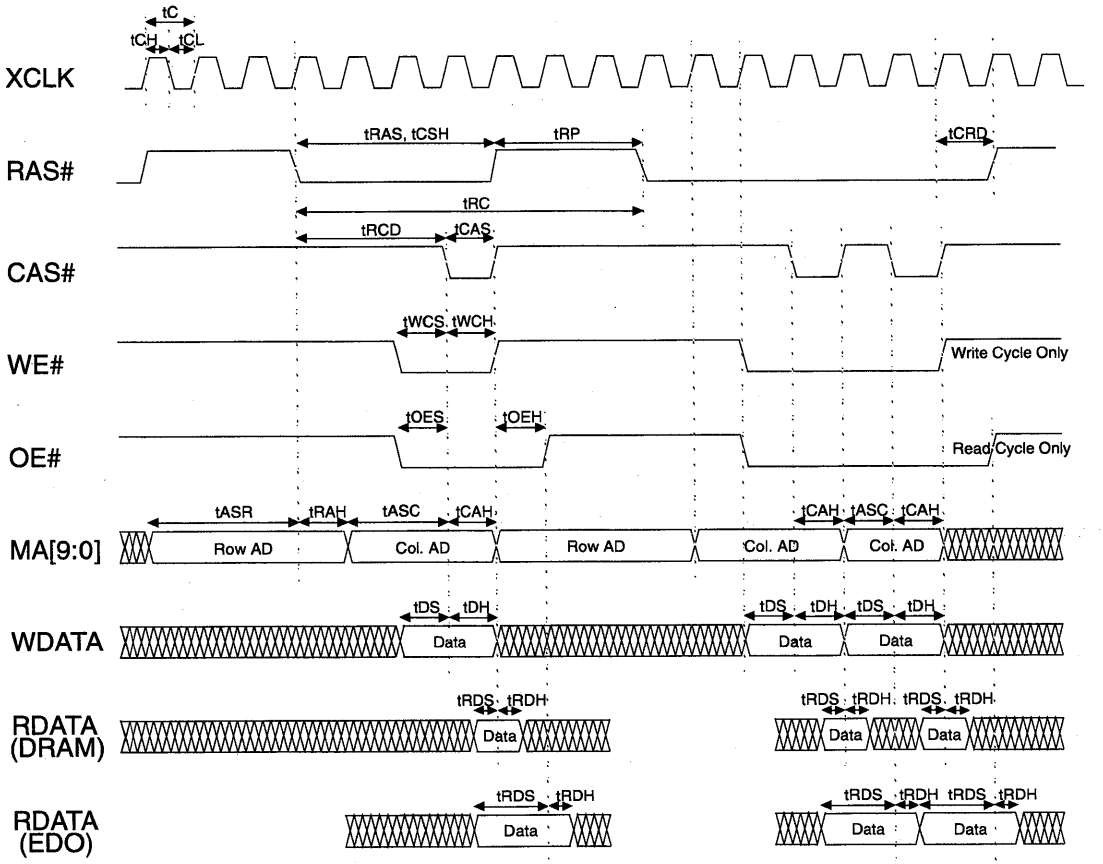


Figure 7-7. DRAM Cycle Timing

Table 7-4 DRAM Interface Cycle Timing Values

Memory Cycle Length	Symbol	Minimum (ns)	Maximum (ns)
Clock Period	tC	12	20
Clock High	tCH	4	-
Clock Low	tCL	4	-
Read Data Setup	tRDS	1	-
Read Data Hold	tRDH	3	-

DRAM/EDO DRAM Controller Values

Table 7-5 DRAM/EDO DRAM Cycle Timing Values

Memory Cycle Length	DRAM Spec.	Register Field in MEM_CNTL or Calc.	MEM_CNTL Bits	Number of XCLKs
Cycle time	tRC	tRP + tRAS		2 to 12
RAS precharge	tRP	MEM_TRP	[9:8]	1 to 4
RAS pulse	tRAS	MEM_TRAS	[18:16]	1 to 8
RAS to CAS (min.)	tRCD	MEM_TRCD	[11:10]	1 to 4
RAS high - CAS high	tCRD	MEM_TCRD	[12]	0 to 1
RAS - CAS high	tCSH	tRCD + 1		2 to 5
CAS Cycle (page mode)	tPC	-		2
CAS precharge	tCP	-		1
CAS pulse	tCAS	-		1
Row address hold	tRAH	-		1
CAS address hold	tCAH	-		1
Output enable setup	tOES	-		≥1
Output enable hold	tOEH	-		≥1
Write command setup	tWCS	-		≥1
Write command hold	tWCH	-		1
Row address setup	tASR	-		≥1
Column address setup	tASC	-		≥1
Write data setup	tDS	-		1
Write data hold	tDH	-		1

7.2.2 Hyperpage EDO DRAM Cycle Timing

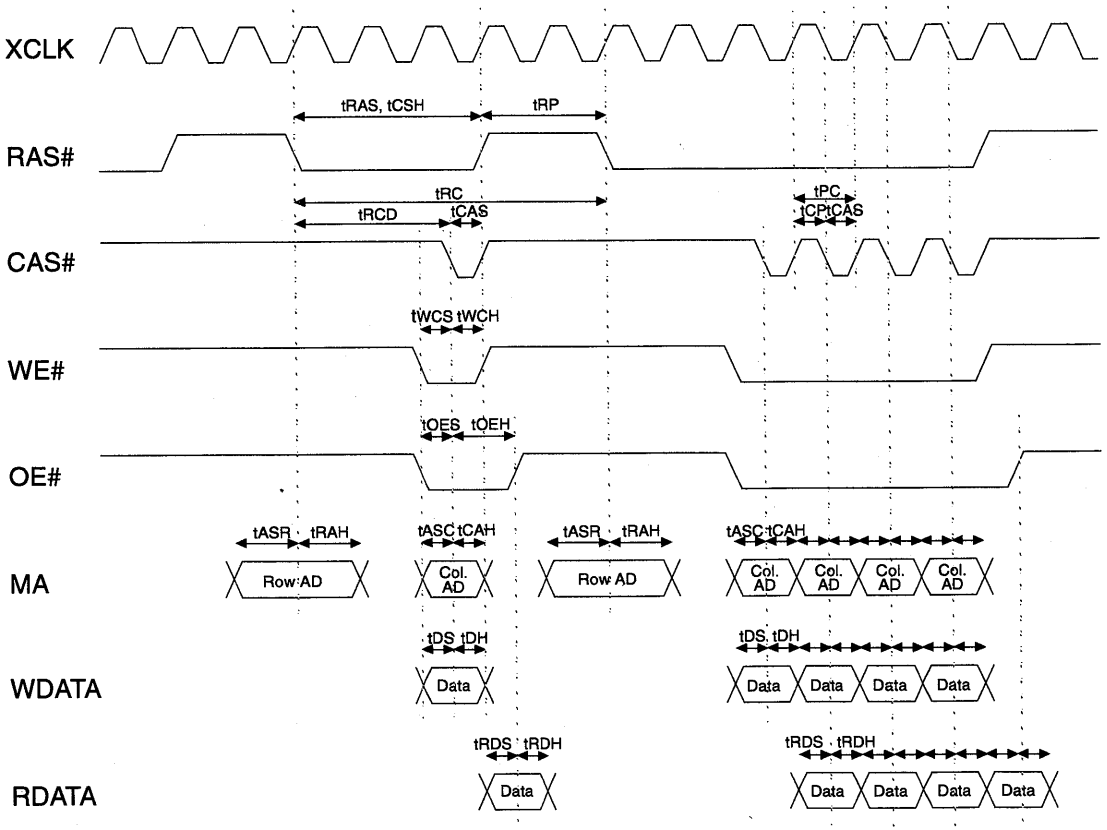


Figure 7-8. Hyperpage EDO DRAM Cycle Timing

Table 7-6 Hyperpage EDO DRAM Timing Values

Memory Cycle Length	DRAM Spec	Min. Time (ns)	Register Field in MEM_CNTL or Calc.	MEM_CNTL Bits
XCLK Period	tC	12		
Cycle time	tRC	2 tC to 12 tC	tRP + tRAS	
RAS precharge	tRP	1 tC to 4 tC	MEM_TRP	9:8
RAS pulse	tRAS	1 tC to 8 tC	MEM_TRAS	18:16
RAS to CAS (min.)	tRCD	1½ tC to 4½ tC	MEM_TRCD + ½	11:10
RAS high - CAS high	tCRD	0 to 1 tC	MEM_TCRD	12
RAS - CAS high	tCSH	2 tC to 5 tC	tRCD + ½	
CAS Cycle	tPC	1 tC	-	
CAS precharge	tCP	½ tC	-	
CAS pulse	tCAS	0.4 tC	-	
Row address hold	tRAH	1 tC	-	
CAS address hold	tCAH	0.4 tC	-	
Output enable setup	tOES	½ tC - 5.0	-	
Output enable hold	tOEH	1 tC	-	
Write command setup	tWCS	½ tC - 5.0	-	
Write command hold	tWCH	0.4 tC	-	
Row address setup	tASR	1 tC	-	
Column address setup	tASC	½ tC - 5.0	-	
Write data setup	tDS	½ tC - 5.0	-	
Write data hold	tDH	0.4 tC	-	

Notes:

- Worst case numbers (max. values) achieved assuming worst case process (setup time): 70 degrees C; 3.0 V; 40 pF on address lines; 28 pF on RAS, WE and OE lines; 14 pF on CAS and data lines.
- Best case numbers (min. values) achieved assuming best case process (hold time): 0 degrees C; 3.6 V; 20 pF on address lines; 28 pF on RAS, WE and OE lines; 7 pF on CAS and data lines.
- Hold and setup time values considered without taking into account transmission line effects of the address, control, and data lines.
- Timing values are provided assuming 1.4 V transition level.

7.2.3 WRAM Cycle Timing

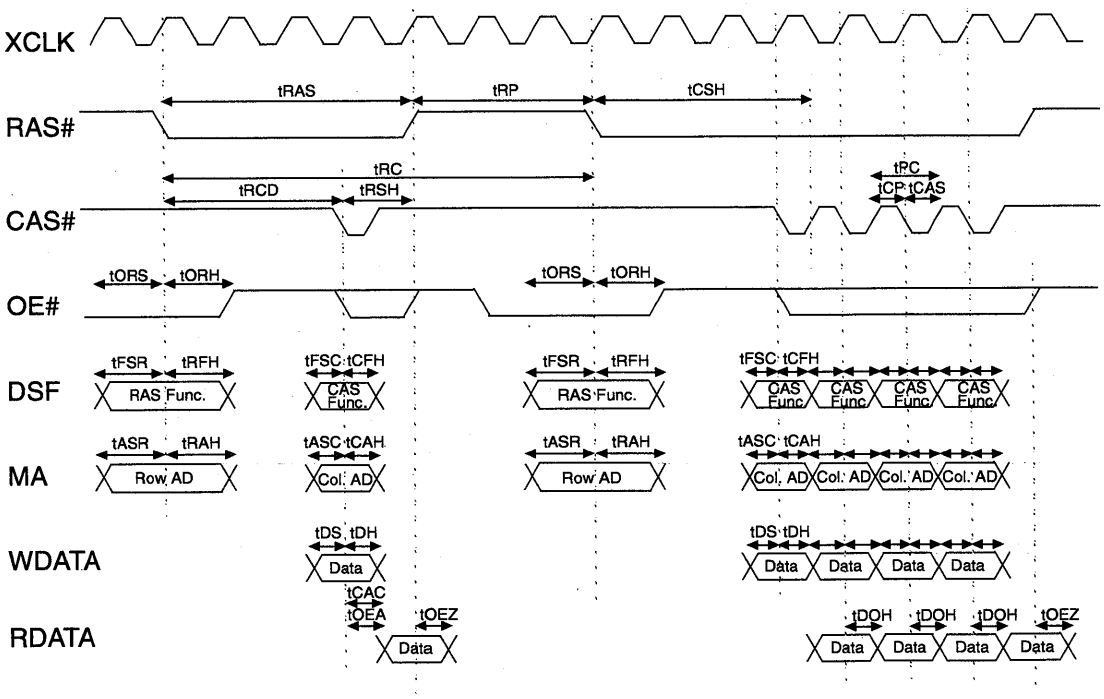


Figure 7-9. WRAM Cycle Timing

Table 7-7 WRAM Interface Timing Values

Memory Cycle Length	DRAM Spec.	Register Field in MEM_CNTL or Calc.	MEM_CNTL Bits	Number of XCLKs
Cycle Time	tRC	tRP + tRAS		2 to 12
RAS precharge	tRP	MEM_TRP	9:8	1 to 4
RAS pulse	tRAS	MEM_TRAS	18:16	1 to 8
RAS to CAS (min.)	tRCD	MEM_TRCD + 1	11:10	2 to 5
RAS hold time	tRSH	MEM_TCRD	12	0 to 1
RAS - CAS high	tCSH	tRCD + ½		2½ to 5½
CAS Cycle	tPC			1
CAS precharge	tCP			½
CAS pulse	tCAS			½
Row address setup	tASR			≥1
Row address hold	tRAH			1
Column address setup	tASC			≥½
Column address hold	tCAH			≥0
DSF setup ref. to RAS	tFSR			≥1
DSF hold ref. to RAS	tRFH			1
DSF setup ref. to CAS	tFCS			≥½
DSF hold ref. to CAS	tCFH			≥0
OE setup ref. to RAS	tORS			≥1
OE hold ref. to RAS	tORH			1
OE setup ref. to CAS	tOSC			2
OE hold ref. to CAS	tOHC			1
Write data setup	tDS			≥½
Write data hold	tDH			≥0

7.2.4 DRAM Refresh Cycle Timing

The Refresh Cycle Timing diagram below applies to DRAM, EDO DRAM, Hyperpage EDO DRAM, and WRAM.

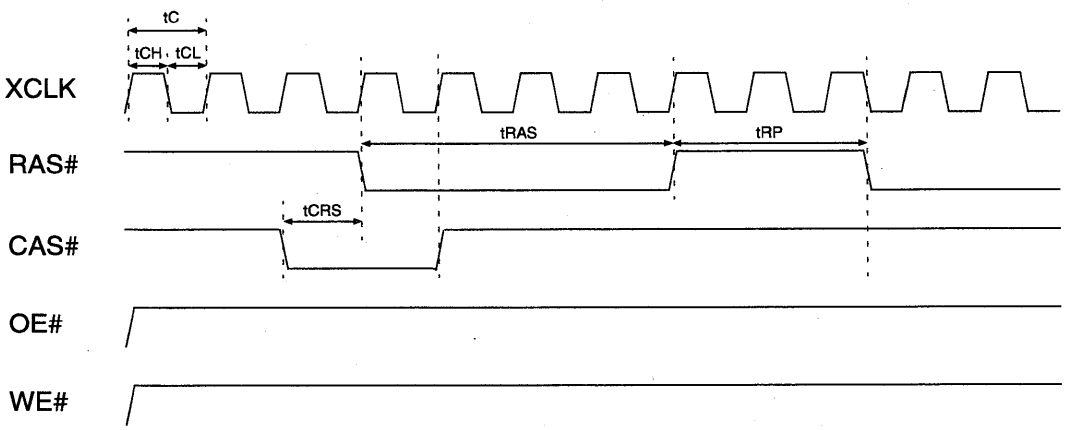


Figure 7-10. Refresh Cycle Timing

Table 7-8 Refresh Cycle Timing Values

Memory Cycle Length	DRAM Spec.	XCLKs (tC)	Register Field in MEM_CNTL or Calc.
Cycle Time	tRC	2 to 12	tRP + tRAS
RAS# precharge time	tRP	1 to 4	MEM_TRP[9:8]
RAS# pulse width	tRAS	1 to 8	MEM_TRAS[18:16]
CAS# to RAS# setup time	tCRS	1	-

7.2.5 SDRAM/SGRAM Cycle Timing

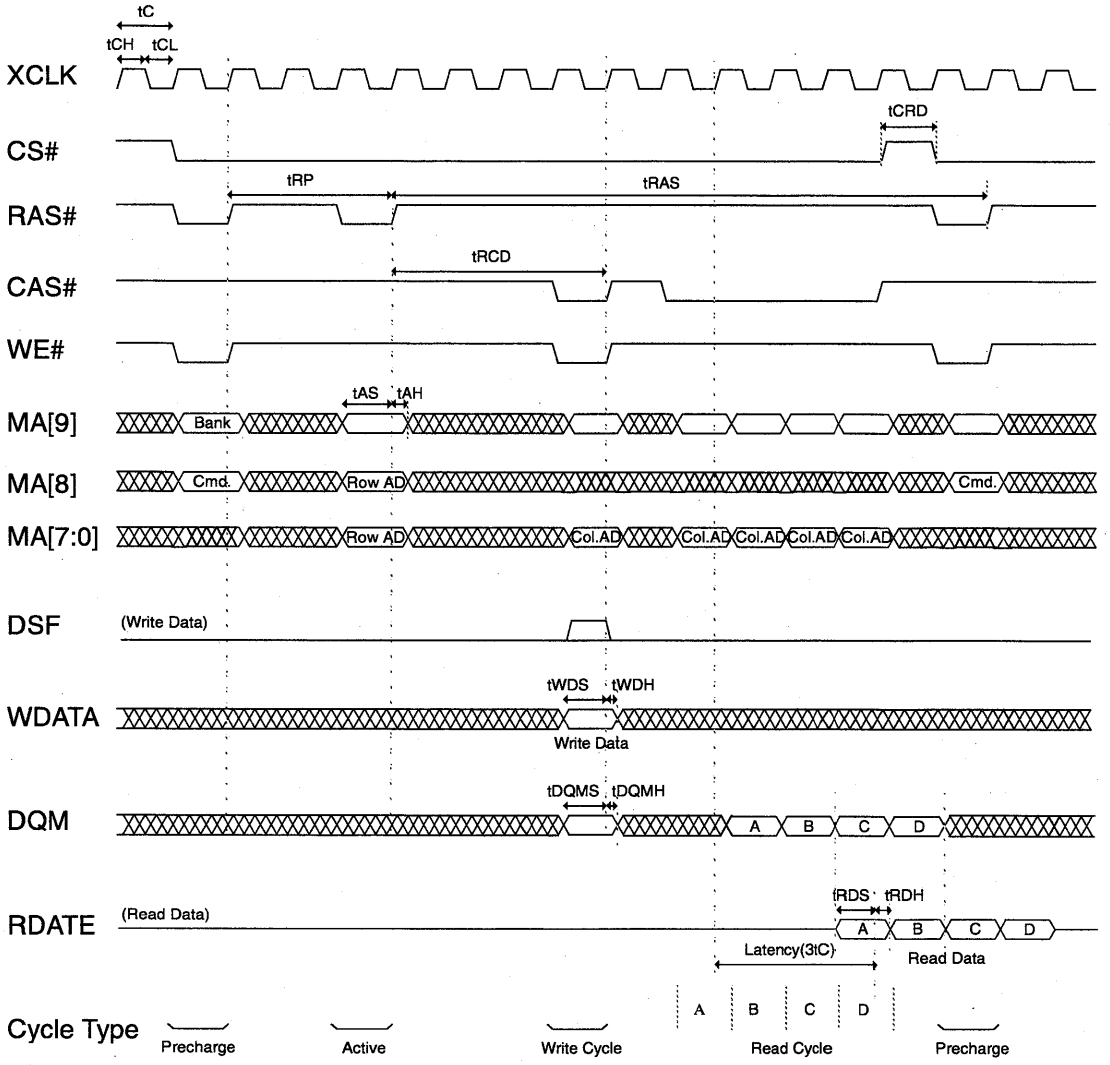


Figure 7-11. SDRAM/SGRAM Cycle Timing

Table 7-9 SDRAM/SGRAM Cycle Timing Values

Parameter	Symbol	Min. (ns)	Max. (ns)	Register in MEM_CNTL
Clock period	tC	10	20	
Clock high time	tCH	4.0	-	
Clock low time	tCL	3.5	-	
Command setup time provided (RAS, CAS, WE, CS, DSF)	tCMS	5.0	-	
Command hold time provided (RAS, CAS, WE, CS, DSF)	tCMH	1.3	-	
DQM setup time provided	tDQMS	5.5	-	
DQM hold time provided	tDQMH	1.2	-	
Address setup time provided	tAS	4.4	-	
Address hold time provided	tAH	1.3	-	
Write data setup time provided	tWDS	3.0	-	
Write data hold time provided	tWDH	2.1	-	
Read data setup time required	tRDS	-0.9	-	
Read data hold time required	tRDH	3.0	-	
Row cycle time	tRC	2 tC	12 tC	MEM_TRP + MEM_TRAS
PRE to ACTV delay	tRP	1 tC	4 tC	MEM_TRP[9:8]
ACTV to PRE min delay	tRAS	1 tC	8 tC	MEM_TRAS[18:16]
ACTV to CMD delay	tRCD	1 tC	4 tC	MEM_TRCD[11:10]
Write recovery time	tWR	1 tC	2 tC	MEM_TCRD[12] + 1
ACTV to ACTV delay	tRRD	2 tC	-	
Block write cycle time	tBWC	2 tC	-	

Notes:

- Worst case numbers (max. values) achieved assuming worst case process (setup time): 70 degrees C, 3.0 V, 45 pF on address and command lines, 30 pF on data and DQM lines.
- Best case number (min. values) achieved assuming best case process (hold time): 0 degrees C, 3.6 V, 5 pF on address and command lines, 3.5 pF on data and DQM lines.
- Hold and setup time values considered without taking into account transmission line effects of the clock, address, command, data and DQM lines.
- Timing values are provided assuming 1.4 V transition level.

7.3 Memory Controller Register Programming Examples

7.3.1 DRAM, EDO DRAM

Table 7-10 DRAM - Values for 15ns Clock Period (67 MHz)

Memory Cycle Length	DRAM Specifications	Register Field in MEM_CNTL or Calc.	Number of XCLKs	Time Provided (nS)
Cycle time	tRC = 104 ns min.	tRP + tRAS	8	120
RAS precharge	tRP = 40 ns min.	MEM_TRP=10	3	45
RAS pulse	tRAS = 60 ns min.	MEM_TRAS=100	5	75
RAS to CAS (min.)	tRCD = 14 ns min., tRCD = 45 ns max.	MEM_TRCD = 01	2	30
CAS high - RAS high	tCRD	MEM_TCRD=1	1	15
RAS - CAS high	tCSH = 40 ns min.	tRCD + 1	3	45
CAS Cycle (page mode)	tPC		2	30
CAS precharge	tCP = 10 ns min.		1	15
CAS pulse	tCAS = 10 ns min.		1	15
Row address hold	tRAH = 10 ns min.		1	15
CAS address hold	tCAH = 10 ns min.		1	15
Output enable setup	tOES = 0 ns min.		≥1	15
Output enable hold	tOEH = 0 ns min.		≥1	15
Write command setup	tWCS = 0 ns min.		≥1	15
Write command hold	tWCH = 10 ns min.		1	15
Row address setup	tASR = 0 ns min.		≥1	15
Column address setup	tASC = 0 ns min.		≥1	15
Write data setup	tDS = 0 ns min.		1	15
Write data hold	tDH = 10 ns min.		1	15

All times are shown to the nearest nano-second (ns).

Table 7-11 Additional MEM_CNTL Register Bits to be Programmed

MEM_CNTL Bits	Register Field Name	Value
5:4	MEM_LATENCY	01 (2 clocks)
7:6	MEM_LATCH	10 (positive edge of XCLK)
13	MEM_TR2W	0 (1 clock delay between read and write)
19	MEM_REFRESH_DIS	0 (enabled)
22:20	MEM_REFRESH_RATE	100 (1 every 1031 XCLK or 512 cycles per 7.9 mS for 67MHz operation)

7.3.2 Hyperpage EDO DRAM

Table 7-12 Hyperpage EDO DRAM (Silicon Magic SM81LC256K16A1-35), XCLK Speed = 83 MHz (12 ns period)

Memory Cycle Length	DRAM Specifications	Register Field in MEM_CNTL or Calc.	Min. Time (ns)	Time Provided (nS)
XCLK Period	tC			12
Cycle time	tRC = 48 ns min.	tRP + tRAS	5 tC	60
RAS precharge	tRP = 17 ns min.	MEM_TRP = 01	2 tC	24
RAS pulse	tRAS = 28 ns min.	MEM_TRAS = 010	3 tC	36
RAS to CAS (min.)	tRCD = 10 ns min.	MEM_TRCD = 00	1 ½ tC	18
CAS high - RAS high	tCRD	MEM_TCRD = 1	1 tC	12
RAS - CAS high	tCSH = 22 ns min.	tRCD + ½	2 tC	24
CAS Cycle	tPC = 12 ns min.		1 tC	12
CAS precharge	tCP = 5 ns min.		½ tC	6.0
CAS pulse	tCAS = 5 ns min.		0.4 tC	4.8
Row address hold	tRAH = 6 ns min.		1 tC	12
CAS address hold	tCAH= 5 ns min.		0.4 tC	4.8
Output enable setup	tOES		½ tC - 5.0	1.0
Output enable hold	tOEH=5 min.		1 tC	12
Write command setup	tWCS=0 min.		½ tC - 5.0	12
Write command hold	tWCH=6 min.		0.4 tC	1.0
Row address setup	tASR=0 min.		1 tC	12
Column address setup	tASC=0 min.		½ tC - 5.0	12
Write data setup	tDS=0 min.		½ tC - 5.0	1.0
Write data hold	tDH=6 min.		0.4 tC	4.8

All times are shown to the nearest nano-second (ns).

Table 7-13 Additional MEM_CNTL Register Bits to be Programmed

MEM_CNTL Bits	Register Field Name	Value
5:4	MEM_LATENCY	01 (2 clocks)
7:6	MEM_LATCH	10 (positive edge of XCLK)
13	MEM_TR2W	0 (1 clock delay between read to write)
14	MEM_CAS_PHASE	0 (CAS low when clock low)
19	MEM_REFRESH_DIS	0 (enabled)
22:20	MEM_REFRESH_RATE	110 (1 every 1250 XCLK or 512 cycles per 7.7 mS for 83 MHz operation)

7.3.3 WRAM

Table 7-14 WRAM (KM423W259A-50), XCLK = 67 MHz, 15ns Clock Period

Memory Cycle Length	DRAM Spec.	Register Field in MEM_CNTL or Calc.	No. of XCLKs	Time Provided(ns)
Cycle Time	tRC=90 ns	tRP = tRAS	7	105
RAS precharge	tRP=35 ns	MEM_TRP = 10	3	45
RAS pulse	tRAS=50 ns	MEM_TRAS = 011	4	60
RAS to CAS (min.)	tRCD=20 ns min	(MEM_TRCD=01) + 1	3	45
RAS hold time	tRSH=15 ns	MEM_TCRD = 1	1	15
RAS - CAS high	tCSH=45 ns	tRCD + ½	3½	52.5
CAS Cycle	tPC=15 ns		1	15
CAS precharge	tCP=5 ns		½	7.5
CAS pulse	tCAS=6 ns		½	7.5
Row address setup	tASR=0 ns		≥1	15
Row address hold	tRAH=6 ns		1	15
Column address setup	tASC=7 ns		≥½	7.5
Column address hold	tCAH=0 ns		≥0	0
DSF setup ref. to RAS	tFSR=0 ns		≥1	15
DSF hold ref. to RAS	tRFH=8 ns		1	15
DSF setup ref. to CAS	tFCS=7 ns		≥½	7.5
DSF hold ref. to CAS	tCFH=0 ns		≥0	0
OE setup ref. to RAS	tORS=0 ns		≥1	15
OE hold ref. to RAS	tORH=8 ns		1	15
OE setup ref. to CAS	tOSC=20 ns		2	30
OE hold ref. to CAS	tOHC=0 ns		1	15
Write data setup	tDS=7 ns		≥½	7.5
Write data hold	tDH=0 ns		≥0	0

Table 7-15 Additional MEM_CNTL Register Bits to be Programmed

MEM_CNTL Bits	Register Field Name	Value
5:4	MEM_LATENCY	01 (2 clocks)
7:6	MEM_LATCH	10 (positive edge of XCLK)
13	MEM_TR2W	1 (2 clock delay between read and write)
14	MEM_CAS_PHASE	1 (CAS low when clock high)
19	MEM_REFRESH_DIS	0 (enabled)
22:20	MEM_REFRESH_RATE	100 (1 every 1031 XCLK or 512 cycles per 7.9 mS for 67MHz operation)

7.3.4 SDRAM/SGRAM

Table 7-16 SGRAM (Hitachi HM5216326-10), XCLK Speed = 100 MHz, CAS Latency = 3

Parameter	SGRAM Specification (ns)	Register Field in MEM_CNTL	Number of XCLKs	Time Provided (ns)
Row cycle time	tRC = 90 min.	tRP + tRAS	9	90
PRE to ACTV delay	tRP = 30 min.	MEM_TRP = 10	3	30
ACTV to PRE mi n. delay	tRAS = 60 min.	MEM_TRAS = 101	6	60
ACTV to CMD delay	tRCD = 30 min.	MEM_TRCD = 10	3	30
Write recovery time	tWR = 20 min.	(MEM_TCRD=1) + 1	2	20

Table 7-17 Additional MEM_CNTL Register Bits to be Programmed

MEM_CNTL Bits	Register Field Name	Value
5:4	MEM_LATENCY	11 (4 clocks, SGRAM CAS latency 3)
7:6	MEM_LATCH	01 (HCLK feedback)
19	MEM_REFRESH_DIS	0 (enabled)
22:20	MEM_REFRESH_RATE	110 (1 every 1250 XCLK or 1024 cycles per 12.8 ms for 100 MHz operation)

Table 7-18 Additional EXT_MEM_CNTL Register Bits to be Programmed

EXT_MEM_CNTL Bits	Register Field Name	Value
0	MEM_CS	1 (allow commands every clock)
9:8	MEM_CLK_SELECT	00 (SD/SGRAM clock from DLL)
11:10	MEM_CAS_LATENCY	11 (SD/SGRAM CAS latency = 3 clocks)
27:24	MEM_GCMRS	0101

The electrical and thermal characteristics described in this document are specific to the *3D RAGE PRO*. Please contact ATI to obtain up-to-date information on how to support all of ATI's graphics controllers, steppings, and foundries in one PCB design.

8.1 Electrical Characteristics

8.1.1 Maximum Rating Conditions

Table 8-1 Maximum Rating Conditions

Item	Value
Supply Voltage, VDDC, VDDR	-0.50V to +7.00V
Supply Voltage, VEE	-0.50V to +7.00V
Input or Output Voltage	-0.05V to ($VEE_{MAX.}$ + 0.05V)
DC Forward Bias Current	-12mA (source) + 24mA (sink)
Storage Temperature (Plastic)	-40°C to 125°C

The extreme values determine the maximum rating conditions and are stress related — operation of the controller at these conditions is not recommended. Ratings are referenced to VDD. Operating outside the ranges may cause permanent damage to the device, and operating close to the maximum rating conditions for extended periods may affect device reliability. Use the recommended ranges below.

8.1.2 Recommended DC Operating Conditions

Table 8-2 Recommended DC Operating Conditions

Item	Value
Operating Supply Voltage (VDDC)	3.3V ±5%
Operating Supply Voltage (VDDR)	3.3V ±5%
Operating Supply Voltage (VEE)	5V ±5%
Operating Case Temperature (TC)	0°C to 80°C

8.1.3 AC Characteristics

Table 8-3 AC Characteristics

Signals	Typical Capacitive Load *
BGROMCS#	10pF
AD[31:0], DEVSEL#, TRDY#, STOP#, INTR#, PAR	50pF
GIO[4:0], BLANK#, PIXEL[7:0], DCLK	25pF
HSYNC, VSYNC	50pF
CAS[1:0], MD[63:0], RAS[1:0], EE[1:0]	25pF
WE[7:0]	15pF
MA[9:0]	45pF
* 4MB, 256Kx16 DRAMs, Feature Connector populated, and through a PCI edge connector.	

8.1.4 DC Characteristics

TTL Interface

Table 8-4 DC Characteristics - TTL Interface

Symbol	Parameter	Condition	Min.	Typical	Max.	Unit
VIL	Low Level Input Voltage	-	-	-	0.8	V
VIH	High Level Input Voltage	-	2.0	-	-	V
VOL	Low Level Output Voltage	IOL=Rated Buffer Current	-	0.2	0.4	V
VOH	High Level Output Voltage	IOH=Rated Buffer Current	2.4	3.3	-	V
VT+	Schmitt Trig. positive threshold	-	-	2.0	2.4	V
VT-	Schmitt Trig negative threshold	-	0.6	0.8	-	V

General

Table 8-5 DC Characteristics - General Interface

Symbol	Parameter	Condition	Min.	Typical	Max.	Unit
IIL	Low level Input Current	VI=VSS	-	-	+1	µA
IIH	High Level Input Current	VI=VCC	-	-	-1	µA
IOZ	Tri-State Output Leakage	VO=0V or VCC	-	-	±10	µA
CIN	Input Capacitance	Freq=1MHz @ 0V	-	4	6	pF
CO	Output Capacitance	Freq=1MHz @ 0V	-	6	-	pF
CIO	Bidirectional I/O Capacitance	Freq=1MHz @ 0V	-	6	10	pF
IKLU	I/O Latch-up Current	V<VSS, V>VCC	500	-	-	mA
VEPO	Electrostatic Protection	C=100pF, R=1.5KΩ	2000	-	-	V

8.1.5 Input/Output Specifications

Table 8-6 Input/Output Electrical Specifications

Pin Name	Type	I_{OL}(min)	I_{OH}(min)	Pull Up/ Pull Down	Tri-State	Interface Level
AD[31:0]	I/O	4mA	-4mA	-	-	5V
C/BE#[3:0]	I/O	18mA	-18mA	-	-	5V
CPUCLK	I	-	-	-	-	5V
DEVSEL#	I/O	18mA	-18mA	-	Yes	5V
FRAME#	I/O	18	-18	-	Yes	5V
IDSEL	I	-	-	-	-	5V
INTR#	O	18mA	-18mA	-	Yes	5V
IRDY#	I/O	18mA	-18mA	-	Yes	5V
PAR	I/O	18mA	-18mA	-	Yes	5V
RESET#	I	-	-	-	-	5V
STOP	I/O	18mA	-18mA	-	Yes	5V
TRDY#	I/O	18mA	-18mA	-	Yes	5V
REQ#	I	-	-	-	-	5V

Table 8-6 Input/Output Electrical Specifications (Continued)

Pin Name	Type	I_{OL}(min)	I_{OH}(min)	Pull Up/ Pull Down	Tri-State	Interface Level
GNT#	I/O	18mA	-18mA	-	Yes	5V
CAS#[1:0]	O	16mA	-16mA	50K PU	Yes	3.3V, 5V Tol.
MA[9:0]	O	8mA	-8mA	50K PD	Yes	3.3V, 5V Tol.
MD[63:0]	I/O	2mA	-2mA	50K PD	Yes	3.3V, 5V Tol.
OE#[1:0]	O	16mA	-16mA	50K PU	Yes	3.3V, 5V Tol.
RAS#[1:0]	O	16mA	-16mA	50K PU	Yes	3.3V, 5V Tol.
WE#[7:0]	I/O	8mA	-8mA	50K PU	Yes	3.3V, 5V Tol.
CS[1:0]	I/O	16mA	-16mA	-	Yes	3.3V, 5V Tol.
R, G, B	A	-	-	-	-	-
RSET	A	-	-	-	-	-
HSYNC	O	18mA	-18mA	-	Yes	3.3V, 5V Tol.
VSYNC	O	18mA	-18mA	-	Yes	3.3V, 5V Tol.
XTALIN	A/I	-	-	-	-	5V CMOS
XTALOUT	A	-	-	-	-	-
EDCLK	I/O	9mA	-9mA	-	Yes	3.3V, 5V Tol.
ESYNC	I/O	9mA	-9mA	-	Yes	3.3V, 5V Tol.
EVIDEO	I/O	9mA	-9mA	-	Yes	3.3V, 5V Tol.
BLANK#	I/O	9mA	-9mA	-	Yes	3.3V, 5V Tol.
DCLK	I/O	18mA	-18mA	-	Yes	3.3V, 5V Tol.
DATA[7:0]	I/O	8mA	-8mA	50K PD	Yes	3.3V, 5V Tol.
ROMCS#	O	4mA	-4mA	-	Yes	3.3V, 5V Tol.
GIO[3:0]	I/O	8mA	-8mA	-	Yes	3.3V, 5V Tol.
GIO4	I/O	4mA	-4mA	-	Yes	3.3V, 5V Tol.
GIO[9:5]	I/O	8mA	-8mA	-	Yes	3.3V, 5V Tol.

8.1.6 DAC Characteristics

All voltages in the table below are referenced to VSS unless specified otherwise.

The Pixel Clock frequency must be stable for a period of at least 20 seconds. after power up (or after a change in Pixel Clock frequency), before proper device operation characteristics are guaranteed.

Table 8-7 DAC Characteristics*

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
-	Resolution	8	-	-	bits	A
VO(max)	Maximum Output Voltage	1.1	-	-	V	A
IO(max)	Maximum Output Current	-	22.05	-	mA	A
-	Full Scale Error	-10	-	+10	%	B, C
-	DAC to DAC Correlation	-2	-	+2	%	A, D
-	Integral Linearity	-0.5	-	0.5	LSB	A, E
-	Rise Time (10% to 90%)	-	-	3	ns	A, F
-	Full Scale Settling Time	-	8	-	ns	A, G, H
-	Glitch Energy	-	60	-	pV-Sec	A, H
-	Monotonicity	-	-	-	-	I
V_{REFM}	Measured Reference Voltage	-6%	1.235	+6%	V	J

* **See Table 8-8 on page 8-7 for PS/2 DAC characteristics**

Notes:

A Tested over the operating temperature range, at nominal supply voltage with an IREF of -2.93mA. (IREF is the level of the current flowing in the RSET resistor).

B. Tested over the operating temperature range, at reduced supply voltage, with a -2.93mA IREF. (IREF is the level of the current flowing in the RSET resistor).

C. Full scale error from the value predicted by the design equations.

D. About the mid point of the distribution of the three DAC's measured at full scale deflection.

E. Linearity measured from the best fit line through the DAC characteristic. Monotonicity guaranteed.

F. Load = 37.5Ω +20pf with IREF = -2.93mA. (IREF is the current flowing in the RSET resistor).

G. From a 2% change in the output voltage until settling to within 2% of the final value.

H. This parameter is sampled, not 100% tested.

I. Monotonicity is guaranteed.

J. V_{REFM} is the measured value of logged data. It is the idealized V_{REF} shifted by 2.9%

8.1.7 Calculating RSET Resistance (DAC Interface)

A precision resistor (with 1% of nominal) is placed between RSET (pin 123) and analog ground (AVSS) to set the full-scale DAC current. This resistance is typically 422Ω for PS/2 applications where the effective impedance is 37.5Ω (doubly terminated 75Ω loads, shown in Figure 8-1). The 422Ω is an acceptable value for RSET with a slightly reduced white level.

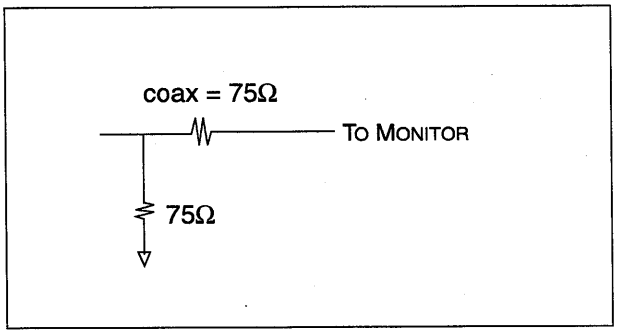


Figure 8-1. PS/2 Example

The required resistor value can be calculated using the formula:

$$\mathbf{RSET\ (\Omega) = (6.22 \times V_{REF} \times \alpha) / I_{OUT}}$$

where: 6.22 is the idealized 8-bit gain constant

V_{REF} is the idealized reference voltage (1.2V)

α is the systematic **composite** skew on idealized V_{REF} and gain constant. It has been empirically determined to be 1.051 from data logging. This amounts to a 5.1% overall correction. (2.9% attributed to V_{REF} and 2.2% to the gain constant)

I_{OUT} is the required DAC full-scale current given by:

$$\mathbf{I_{OUT} = (V_{WHITE} - V_{BLACK}) / Z_{EFF}}$$

For: $V_{WHITE} = 0.7V$

$V_{BLACK} = 0V$

$Z_{EFF} = 37.5\Omega$

$I_{OUT} = 0.7V - 0V / 37.5\Omega = 0.0186A$

Defining RSET in this fashion allows for a one-time compensation for the systematic skew due to shifts on both V_{REF} and the gain constant on the output white level by adjustment of α.

The variation in α has been set to be 10%, of which 6% has been attributed to the bandgap (V_{REFM} = 1.2 x 1.029 ± 6% = 1.235 ± 6%), and the rest (4%) to the variation of the gain constant. Hence,

I_{OUT} max = 18.6mA x 1.1
I_{OUT} min = 18.6mA x 0.9

PS/2 Example:

$$\text{RSET } (\Omega) = (6.22 \times V_{REF} \times \alpha) / I_{OUT}$$
$$= 6.22 \times 1.2 \times 1.051 / 0.0186$$
$$= 422\Omega$$

Table 8-8 PS/2 DAC Characteristics*

Parameter	Min.	Typ.	Max.	Unit
V_{WHITE}	630	700	770	mV
I_{OUT}	-10%	18.6	+10%	mA

* Values obtained using 37.5Ω load, 422Ω (± 1%) RSET with 8-bit white level.

8.1.8 Analog Output Specification

Conceptually, each 8-bit DAC can be viewed as two current sources connected in parallel. Each current source is controlled independently as shown below.

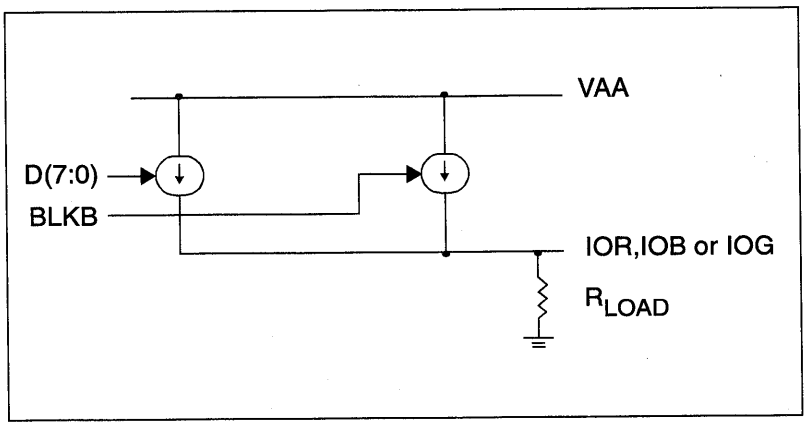


Figure 8-2. Analog Output (DAC)

With a 75Ω doubly-terminated load, V_{REFM} = 1.235V, and RSET = 422Ω, PS/2 levels are shown below, with pedestal current set to 7.5 IRE.

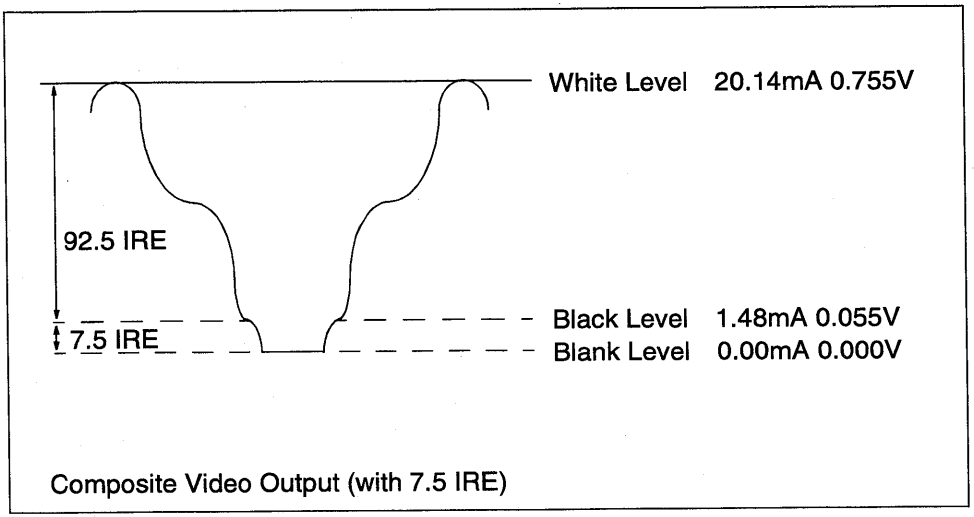


Figure 8-3. Analog Output (Composite)

8.2 Thermal Characteristics

The thermal operation characteristics of the chip depend on the board it is mounted on. The tables below present the values of θCA (case-to-ambient thermal resistance) and TA*max* (maximum ambient temperature) for different airflows over the chip.

Table 8-9 Single-layer Board

Airflow (m/s)	0	0.5	1.0	2.0	3.0
θCA(°C/W)	21.0	15.8	14.5	11.9	11.3
TA*max*(°C)	28	44	49	57	59

Table 8-10 Multi-layer Board with Ground Plane

Airflow (m/s)	0	0.5	1.0	2.0	3.0
θCA(°C/W)	17.6	14	12.5	10.4	10.0
TA*max*(°C)	39	50	55	62	63

8.2.1 Maximum Ambient Temperature

Typical maximum ambient temperatures (TA*max*) can be derived from the maximum case temperature (TC*max*), power dissipation, and case-to-ambient thermal resistance (θCA) as follows:

$$TA_{max} = TC_{max} - P * \theta CA$$

Power dissipation (**P**) range varies with different display frequencies but is typically between 1.0W to 2.0W when chip is operating at nominal VDD. Case temperature (**TC**) may be measured in any environment, and should be taken at the center of the top surface of the device.

8.2.2 Junction Temperature

The junction-to-case thermal resistance (θJC) of this device is approximately 6.7°C/W. Junction temperature (TJ) may be calculated as follows:

$$TJ = (\theta JC + \theta CA) * P + TA$$

8.3 Power and Case Temperature Measurements

The following table presents the results of *3D RAGE PRO* ASIC and memory (4M SGRAM) power consumption and case temperature measurements. Since the power and temperature depends on the activity inside ASIC, the measurements are done in three categories: 2D demo on; 2D demo off; and 3D demo on.

Intel A2 Motherboard is used as a test station, CRT display (ISR 10011-035) - as an output device.

Table 8-11 Power Consumption and Case Temperature

Operation Conditions	ASIC		SGRAM (4M)
	Power	Case Temp.	
Nominal: 640x480x32bpp at 75Hz Both 2D and 3D demo off.	1.1 W	45 °C	0.5 W
Extreme: 1600x1200x16bpp at 85Hz 3D demo on.	2.6 W	66 °C	0.8 W

Note: room temperature was 23.9 °C.

8.4 Physical Dimensions

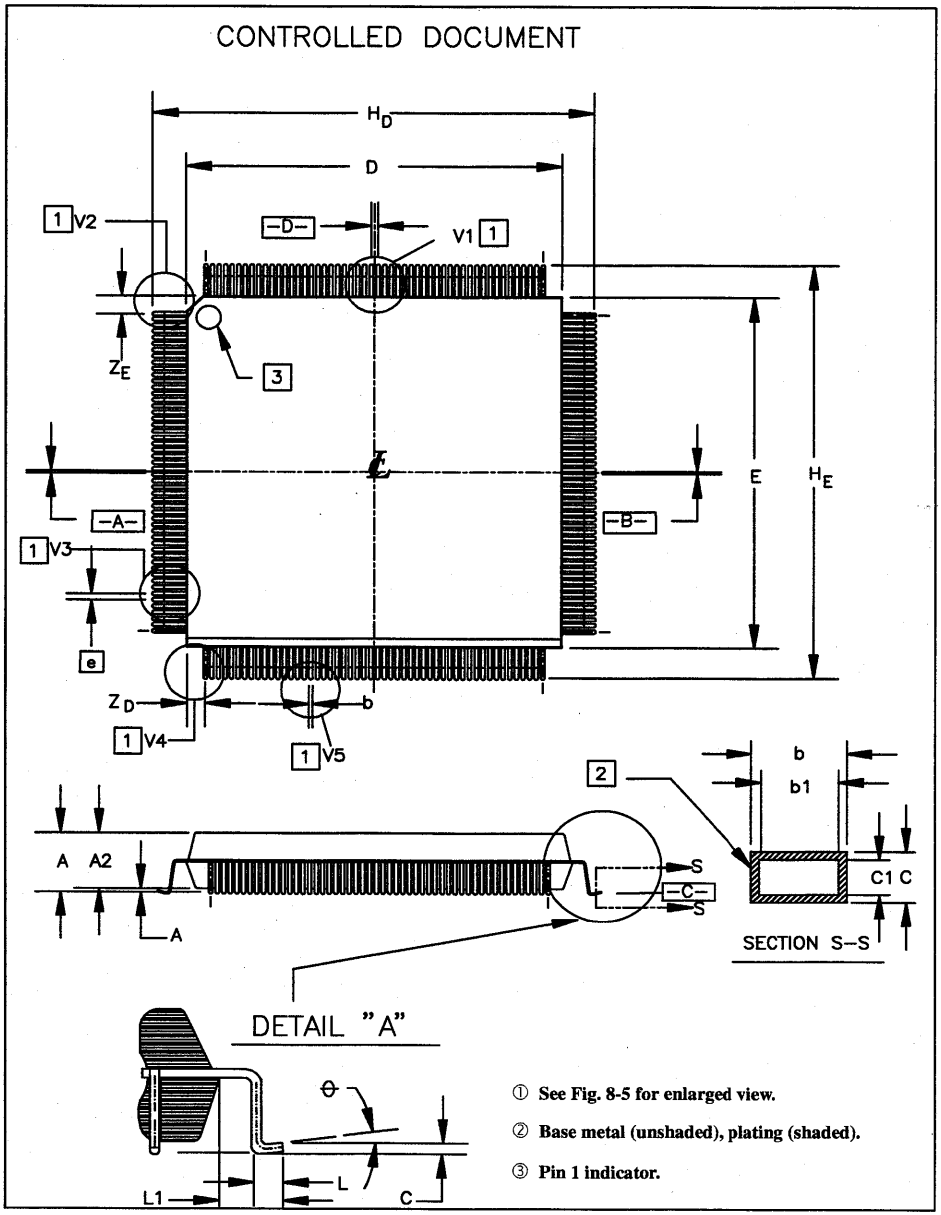


Figure 8-4. Controller Physical Dimensions (PQFP Package)

Table 8-12 PQFP Package Physical Dimensions

Ref.	Millimeters		
	Typical	Min.	Max.
A			4.20
A1		0.25	
A2		3.20	3.70
b		0.15	0.30
b1		0.15	0.26
C		0.10	0.20
C1		0.10	0.16
D		27.80	28.20
E		27.80	28.20
e	0.50		
HD		30.20	31.00
HE		30.20	31.00
L		0.40	0.60
L1	1.30		
ZD	1.25		
ZE	1.25		
θ	-	0*	8*

* θ is measured in degrees.

Notes:

- This package may include a heat spreader or copper slug.
- This layout represents packages assembled free-leaded at subcontractor assembly sites.

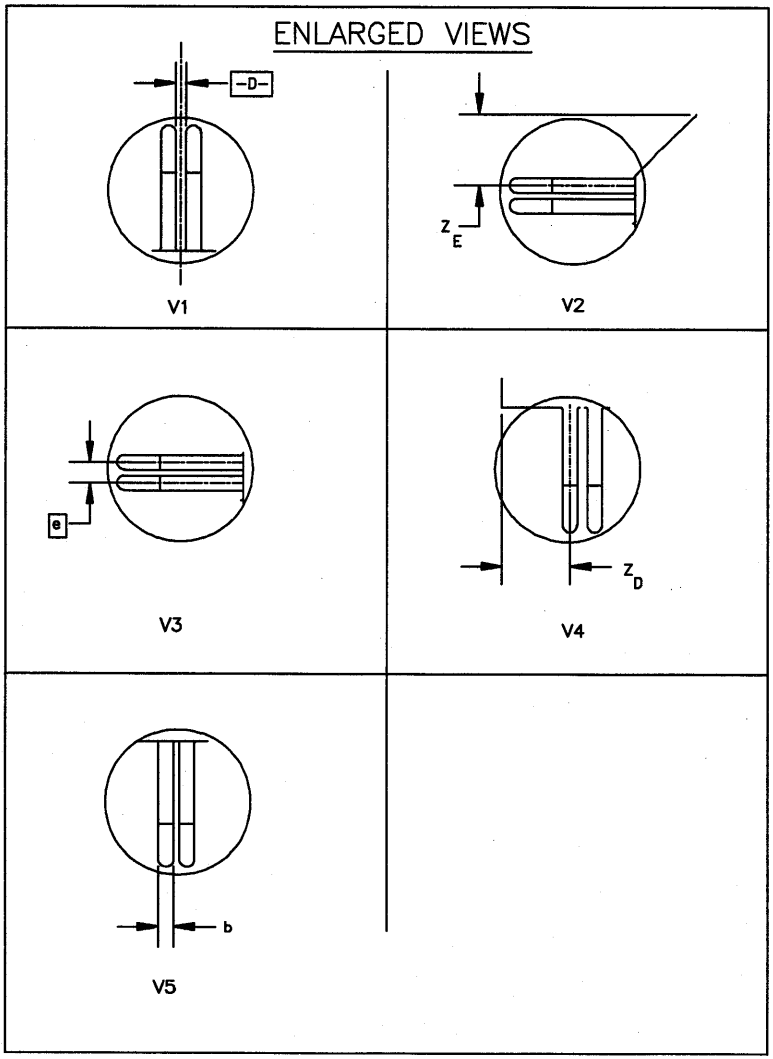


Figure 8-5. Enlarged View of Figure 8-4

Package outline PBGA 27x27 - 256&256 +16

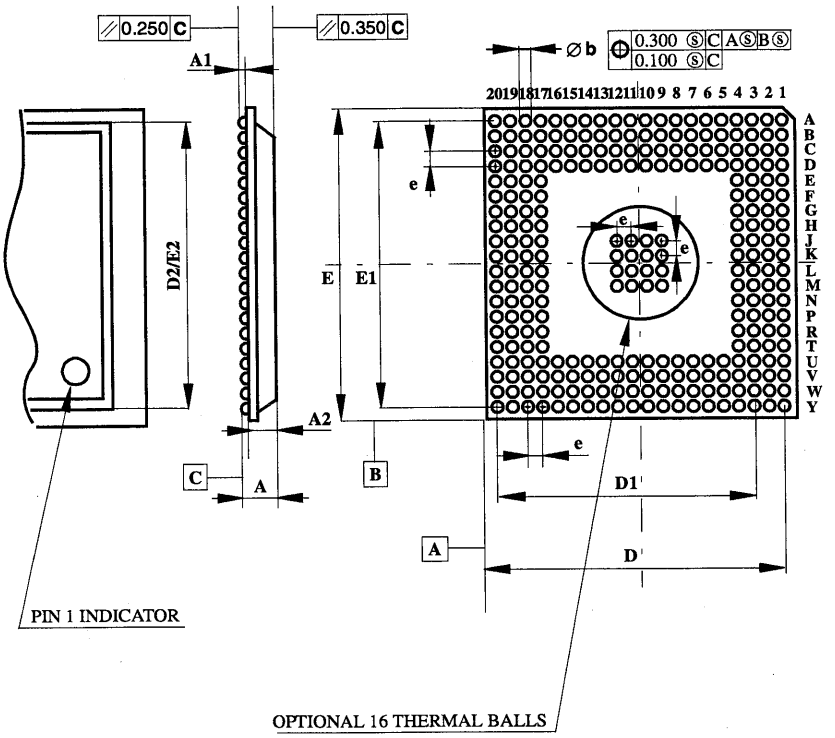


Figure 8-6. Controller Physical Dimensions (BGA Package)

Table 8-13 BGA Package Physical Dimensions

Ref.	Millimeters		
	Typical	Min.	Max.
A		2.125	2.595
A1		0.50	0.70
A2		1.625	1.895
b		0.60	0.90
D	27.00	26.82	27.18
D1	24.13 BASIC		
D2		23.90	24.10
e	1.27 BASIC		
E	27.00	26.82	27.18
E1	24.13 BASIC		
E2		23.90	24.10

Notes:

- Drawing BGA 27x27 finished 14090116-004
- Reference document JEDEC M0151

8.5 Environmental Requirements

8.5.1 Ambient Temperature

Operation: 50 °F to 122 °F (10 °C to 50 °C)

Storage: 32 °F to 162 °F (0 °C to 70 °C)

8.5.2 Relative Humidity

Operation: 5% to 90% non-condensing

Storage: 0% to 95%

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Appendix A
Layout Considerations

A.1 AGP Signal Routing

AGP signals must be carefully routed on the graphics card to meet the timing and signal quality requirements set out in the AGP Interface Specification Technical Manual, Rev.1.0. This chapter presents some general guidelines which should be followed. These guidelines are also covered in the Accelerated Graphics Port Platform Design Guide, Rev.1.0. The trace lengths mentioned are the guidelines only, and it is the responsibility of the board designer to simulate the routing in order to verify that the specification is met. All trace lengths are defined for a nominal trace impedance of 65Ω with a variation of +/-15Ω.

A.1.1 Trace Length

Signal Trace length on the AGP board should not be greater than 3.00". This requirement is derived from the flight time budget of 0.7ns for the add-in card.

CPUCLK signal length should be carefully designed to match the 0.6 ns +/-0.1ns flight time requirement in AGP specification. This trace length has to be calculated based on the special implementation requirements: number of layers, thickness of layers, width of trace, etc. A simplified formula can be used to define the propagation delay

$$\textit{Tprop (ps/in.)} = 85\sqrt{(0,475\varepsilon r + 0,67)}$$

where εr is the relative permeability of the substrate.

A.1.2 AGP signal grouping and Routing

AD_STB strobe signal is grouped with the address signals AD(15:0) and C/BE[1:0] and should be routed in the middle of the above address group.

AD_STB1 strobe signal is grouped with the address signals AS(31:16) and C/BE[2:3] and should routed in the middle of the above address group.

SB_STB strobe signal is grouped with the side band address signals SBA(7:0) and should routed in the middle of the above address group

Strobe signals should be within +/-0.5" of their respective groups. The pin assignment of the AGP groups on the *3D RAGE PRO* is such that traces can be easily laid out to even tighter requirements.

Example: If strobe signal AD_STB0 = 2.5" then signal group AD(15:0), C/BE[1:0] should be from 2.0" to 3.0" in length.

Some rules will be applied to AD(31:16), SBA(7:0) and their strobes AD_STB1, ST_STB respectively.

A.1.3 Signal Guarding and Trace Pitch

The following are the time critical signals which have to be guarded in order to minimize crosstalk - AD_STB0, SB_STB and PCI clock. It is intended to have a ratio of 1:4 between signal Trace Width and Trace Pitch dimensions for the guarded signals. All other signals Width to Trace pitch ratios should be minimum 1:2.

A.2 PCB Layout Considerations

Digital circuits can easily generate large ground current spikes that appear as an increase in the circuit's noise floor. You can achieve superior operation of the graphics subsystem when the coupled noise at the PLL and DAC supplies and references are minimized. The following rules of thumb adhere to the guiding premise that ground currents for digital circuits should be adequately bypassed and kept away from sensitive circuit areas and analog supplies.

- Keep digital signals away from analog signals.
- Keep digital components and wires as far away from analog sections as possible. Avoid routing digital signals through analog sections.
- Keep sensitive nets short by placing analog components close to the chip, and short wires over their respective planes. These are RSET, XTALIN, and XTALOUT.
- All power pins need by-pass capacitors placed as close to the pins as possible.
- On 4-layer designs, position the ground plane closest to the component side and the power plane closest to the solder side.
- All ground nets, VSS, AVSS, and PVSS should be joined together at one location as close to the card edge connector as possible.
- Use a low impedance ground, i.e., a continuous ground plane.
- Provide separate filtered power supplies for analog functions.
- Use capacitors and ferrite beads on RGB signals to reduce EMI for FCC requirements.
- Apply PCI specifications to routing traces from the PCI bus.

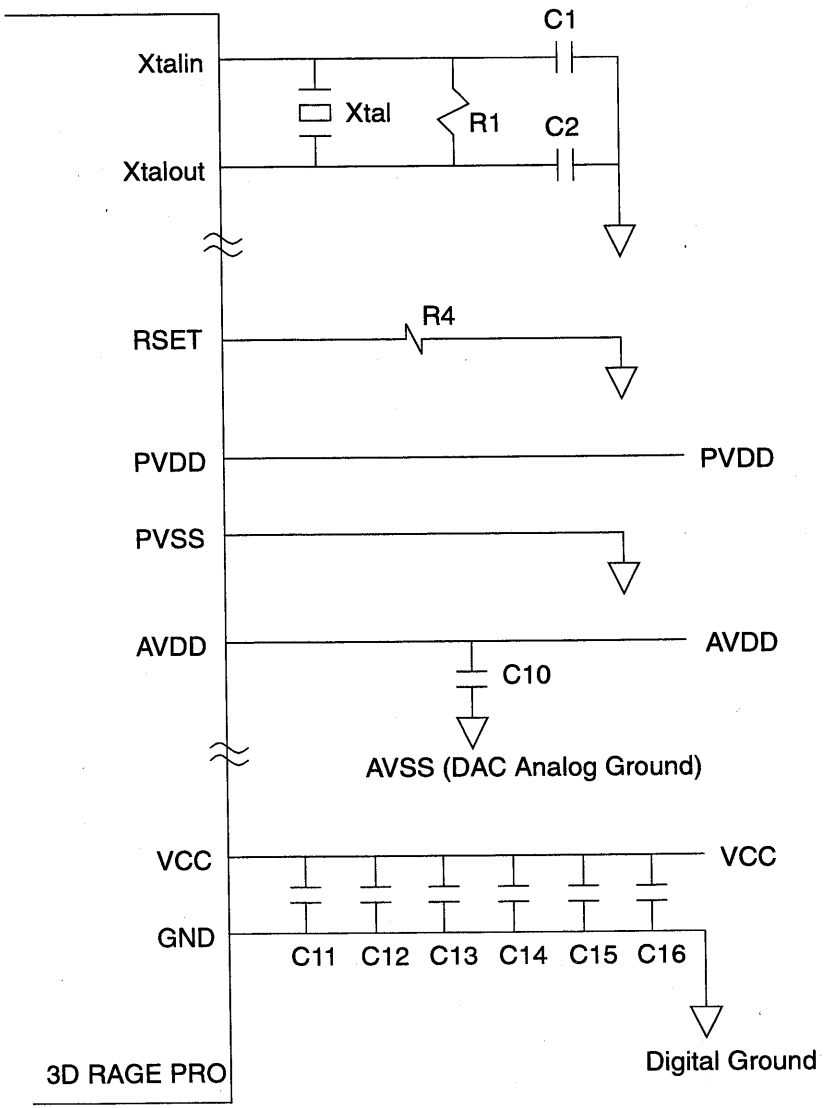

Figure A-1. PCB Layout Component Diagram

A.3 Routing and Layer Assignments

A.3.1 Star Grounding

Star grounding minimizes common mode voltages caused by the noise currents traveling through common mode impedances. Common mode impedance is created when long tracks are snaked around a board. A voltage can be developed at the point on the track (away from the common ground or supply point) which a primary current flows into. If this point is then used to provide a common ground point connection for a second macro, the voltage generated by the primary current will be superimposed on the ground of the second macro even if it (second macro) does not sink or source any current.

Star grounding is an idealized grounding topology whereby macros are provided a separate and direct path to a common physical point. This point is tied to a very low impedance path directly to the supply return. In this manner, no common mode impedance can be developed between macros and no noise coupling is possible. When correctly implemented, the Star point should physically appear to have many wires leading away from it to respective macros which rely on the point to provide a potential that is common to them all.

All macros that attach to common analog grounds and supplies should have wide, short, low impedance paths to "star points". Conceptually, this should be a wire to the power supply but practicality restricts it to a point on the circuit board.

On the graphics controller, supplies are logically separated into three pairs:

- AVSS/AVDD
- PVSS/PVDD
- VSS/VCC

As the only one physical ground return exists, AVSS, PVSS, and VSS should be connected together to one point as close to the card edge connector as possible.

A.3.2 Local Bypassing

By bypassing the supply pairs (AVSS/AVDD, PVSS/ PVDD, and VSS/VCC) we minimize residual common mode currents that could couple in noise between macros in the common mode impedances that cannot be eliminated. (e.g., the wire connecting the power supply to the board).

A.3.3 Signal Referencing

Signal referencing on the graphics controller is important since not all the signals are ground referenced. The significance is in the difference between the input node and the node to which it is referenced. For nodes which handle primarily DC and LF (low frequency) information, a high-pass function in the form of either guard ring or guard island can be formed from adjacent tracks and underlying layers, respectively.

Numerics

A

B

C

D

E

F

T

U

V

W

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