ProMotion-6410™

Advanced
MultiMedia User Interface
Accelerator
Databook

Alliance Semiconductor

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1. Introduction

Features

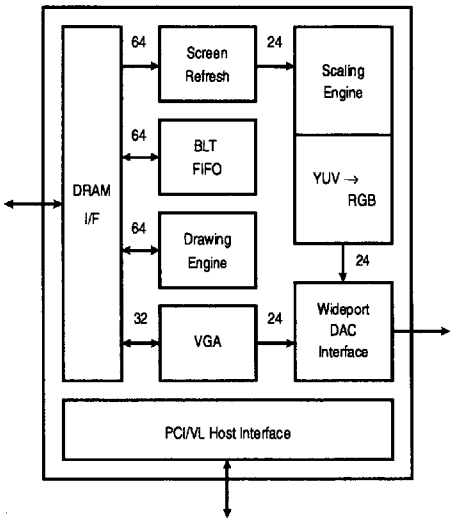
- **Fast 64-bit GUI accelerator**
  - Optimized 64-bit BLT/pattern engine
  - Color expansion
  - Line draw, Ditherfill™, quick-start
- **Smooth scaled video at 30 fps**
  - Hardware scaling up to full screen
  - On-chip YUV to RGB conversion
  - Intel/Microsoft DCI support
  - Video+graphics in 1MB buffer
- **BetterHalf™ memory saving technology**
- **VESA® Advanced Feature Connector**
- **Glueless PCI/VL interface**
  - PCI™ Bus v2.0
  - VESA VL-bus™
- **Efficient memory-mapped addressing**
- **Fast interleaved DRAM interface**
  - 213MB/second peak bandwidth
  - 1MB, 2MB, 4MB display memory
  - ×4, ×8, ×16 DRAM support
- **VESA DPMS power management**
- **Programmable resolution to 1600 × 1200**

	256 colors	32K/ 64K colors	16M colors
1600×1200	✓		
1280×1024	✓	✓*	
1152×864	✓	✓	
1024×768	✓	✓	✓*
800×600	✓	✓	✓
640×480	✓	✓	✓

*Interlaced

- **Flexible 8/16-bit DAC support**
  - Up to 160 MB/sec pixel transfer
- **Full VGA & BIOS compatibility**

Block diagram



Overview

ProMotion-6410 is a member of Alliance Semiconductor's ProMotion™ family of high-performance **MultiMedia User Interface** (MMUI) accelerators. It incorporates a powerful Windows™ graphical user interface accelerator engine, unique motion video acceleration hardware, an efficient memory-mapped PCI/VL interface, and a fully compatible VGA controller, all in a single integrated PQFP package.

A optimized **64-bit accelerator engine** and highly tuned memory interface give the 6410 superior performance in a low-cost DRAM-based accelerator. The large available memory bandwidth, along with efficient driver software, means uncompromising GUI performance.

The chip's unique **multimedia acceleration engine** enables low cost, high quality motion video playback. The engine includes an on-chip color space converter to accelerate decompression, and a hardware scaler with proprietary anti-blocking circuitry to scale continuously from native size up to full screen without loss of performance. The engine delivers smooth, 30 fps display of motion video data at SIF resolution under DCI, Video for Windows™, Indeo™, and other video applications and codecs.

Software drivers

- **High Performance Windows™ 3.X**
  - Flat model optimized drivers
  - 256, 32K, 64K, 16M color support
  - Multi-resolution 640×480 up to 1600×1200
- **Microsoft® DCI motion video**
  - Codec-neutral, multi-vendor standard
  - MPEG-1, Indeo™, Cinepak, TrueMotion
- **Microsoft Video for Windows™**
- **AutoDesk® ADI**
  - AutoCAD®, AutoShade®, 3D Studio
- **WordPerfect® 6.0**
- **OS/2™ Warp, 2.X, EnDIVE**
- **Windows NT™ 3.5**
- **NeXTStep™**
- **SCO™ UNIX®**

→ ***Complete, High-performance, Robust***

Alliance supports the ProMotion family with high-quality flat model optimized driver software. ProMotion drivers take full advantage of ProMotion-6410 hardware and the latest software technology to accelerate real performance of real applications, from word processing and spreadsheets to the most demanding CAD programs and multimedia software.

The ProMotion driver set accelerates the operating environments, graphics-intensive software, and motion video applications listed at left. With 100% VGA register compatibility, ProMotion controllers can also run standard DOS and VBE-compatible applications directly without driver software.

Source code to ProMotion drivers is available to permit customization and differentiation.

VGA BIOS

- **Industry standard Phoenix® BIOS**
- **100% IBM® compatible**
- **VESA support**
  - DPMS power management
  - BIOS extensions
  - DDC
- **Menu-driven configuration management**
- **Binary size under 32KB**

→ ***Compatible, User-friendly***

The ProMotion-6410 chip controls an optional VGA BIOS ROM for add-in card applications. Binary and source code for the Phoenix® BIOS are available from Alliance.

Manufacturing package

- **Reference PCB designs**
- **OEM software utilities**
- **Customer software utilities**

→ ***Full customer support***

ProMotion reference designs, OEM tools, and application notes reduce time-to-market. Alliance's OEM support and quality standards, developed over years as a high-volume system supplier to the PC industry, meet the strictest requirements.

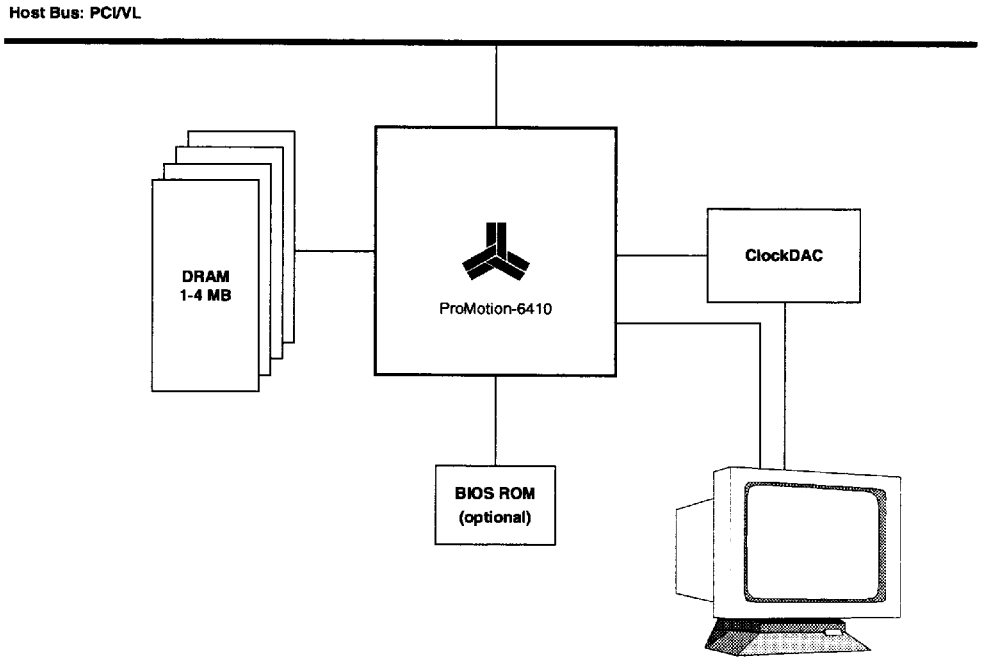
No-cost motion video™

- **Motion video application explosion**
  - Entertainment
  - Education
  - Training
  - Communication
- **Specialized requirements**
  - Color space conversion
  - vWindow™ scaling and pixel interpolation
  - 3X throughput by offloading CPU

→ ***30 fps full-screen with popular codecs***

Just as the shift from text-based to graphical user interface created a need for GUI acceleration, today's shift to multimedia user interface has created a need for motion video acceleration. Customers investing in new hardware need the ability to run current and future software titles. Common software codecs require a small set of specialized operations which are CPU-intensive but can be accelerated with hardware. For a typical stored-video codec like Indeo, off-loading color space conversion and scaling from the host CPU can improve throughput threefold, increasing frame rates and eliminating jerky dropped frames.

System block diagram



2. Functional description

2.1. Graphics accelerator

The ProMotion-6410 MMUI accelerator includes an ultra-high-performance graphics controller designed for demanding truecolor, hi-color, and pseudocolor GUI and CAD applications. A dedicated BLT engine maximizes performance of host-to-screen and screen-to-screen operations. A separate drawing engine efficiently handles pattern fills, text rendering, lines and polygons. Advanced features include:

- **Color DitherFill™**
- **Source and destination transparency**
- **Strip draw**
- **Quick-start and auto-update capability**
- **Linear memory access**
- **Mono-to-color expansion**
- **Line draw**
- **Short-stroke vectors**
- **Clipping**
- **Hardware cursor**

2.2. Motion video accelerator

An integrated motion video accelerator enables popular software codecs to achieve 30fps full-screen playback using a standard inexpensive truecolor DAC, and with no additional off-chip hardware. ProMotion-6410 accomplishes this feat by off-loading the CPU-intensive tasks of **scaling** and **color space conversion**, and by minimizing the memory bandwidth required for display of decompressed video data.

The chip manages a **hardware motion video window**, the vWindow™, whose data is stored in an off-screen area of the standard frame buffer memory. When displaying the vWindow, the controller stretches by programmable X and Y factors ranging from 1.01 to 255.0; proprietary interpolation and anti-blocking circuitry enhances the quality of scaled low-resolution images. Motion video data may be in pseudo-color, RGB, or YUV format (4:2:2, 4:1:1, or 4:0:0). ProMotion-6410 converts YUV data to RGB "on the fly" for display by a standard low-cost DAC.

Because YUV format is more compact than truecolor RGB, and because each motion video frame is sent across the host bus at its unscaled resolution, the host sends only the minimum required data across the system bus. Because ProMotion-6410 does scaling on the fly, it reads only the minimum required data from the frame buffer for each screen update, making the best possible use of available bandwidth. ProMotion's innovative architecture removes bandwidth bottlenecks to display multimedia data at its full speed.

2.3. VGA controller

A fully register-compatible Super VGA controller in the ProMotion-6410 chip supports all monochrome and 4-bit packed and planar modes. The controller is reverse-compatible to MDA, CGA, and IBM VGA standards as well. Super VGA modes conform to VESA standards.

VESA No.	Screen format	Display mode
0,1	360 x 400	Text
2,3	720 x 400	Text
4,5	320 x 200	Graphics
6	640 x 200	Graphics
7	720 x 400	Text
D	320 x 200	Graphics
E	640 x 200	Graphics
F	640 x 350	Graphics
10	640 x 350	Graphics
11	640 x 480	Graphics
12	640 x 480	Graphics
13	320 x 200	Graphics

Figure 2.4.1. Glueless PCI/ROM interface

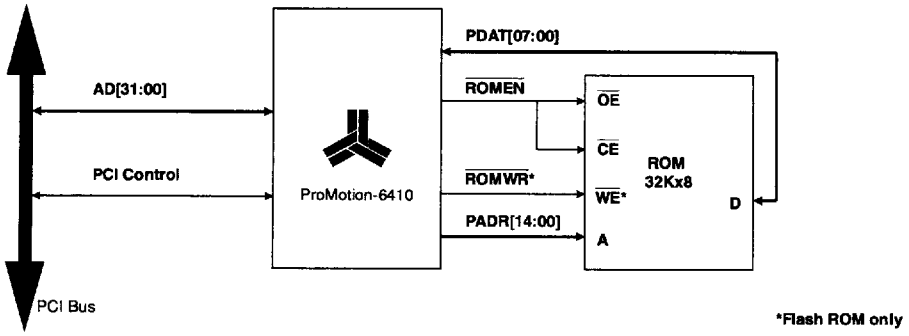
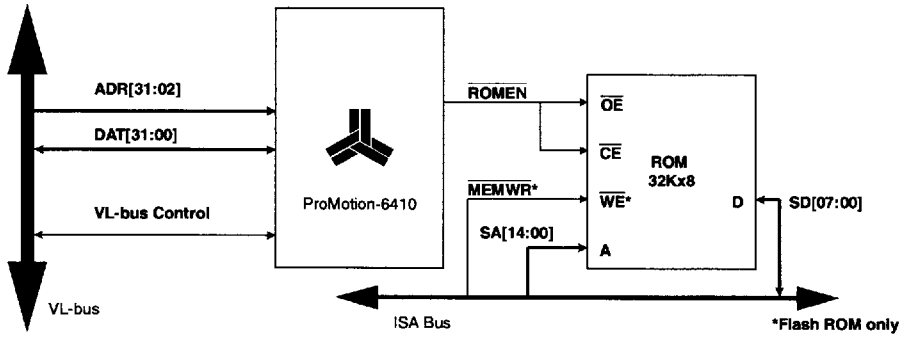


Figure 2.4.2. Glueless VL-bus/ROM interface



2.4. PCI/VL host interface

The ProMotion-6410 interfaces directly to **PCI Bus** v2.0 or to VESA **VL-bus**, without external glue logic. A configuration strap on MD[27] selects host interface mode. If this line is pulled LOW during chip reset, the chip configures itself in PCI mode, with full support for the v2.0 specification. If the configuration strap is undriven or pulled HIGH, the chip configures itself in VL-bus mode.

Memory-mapped command registers for the ProMotion-6410 graphics engine make common operations fast. A optimized **command FIFO** further improves performance. Writes to the frame buffer memory and to chip registers are buffered in the FIFO, transparently to software, so the host processor can continue execution.

2.5. ROM BIOS interface

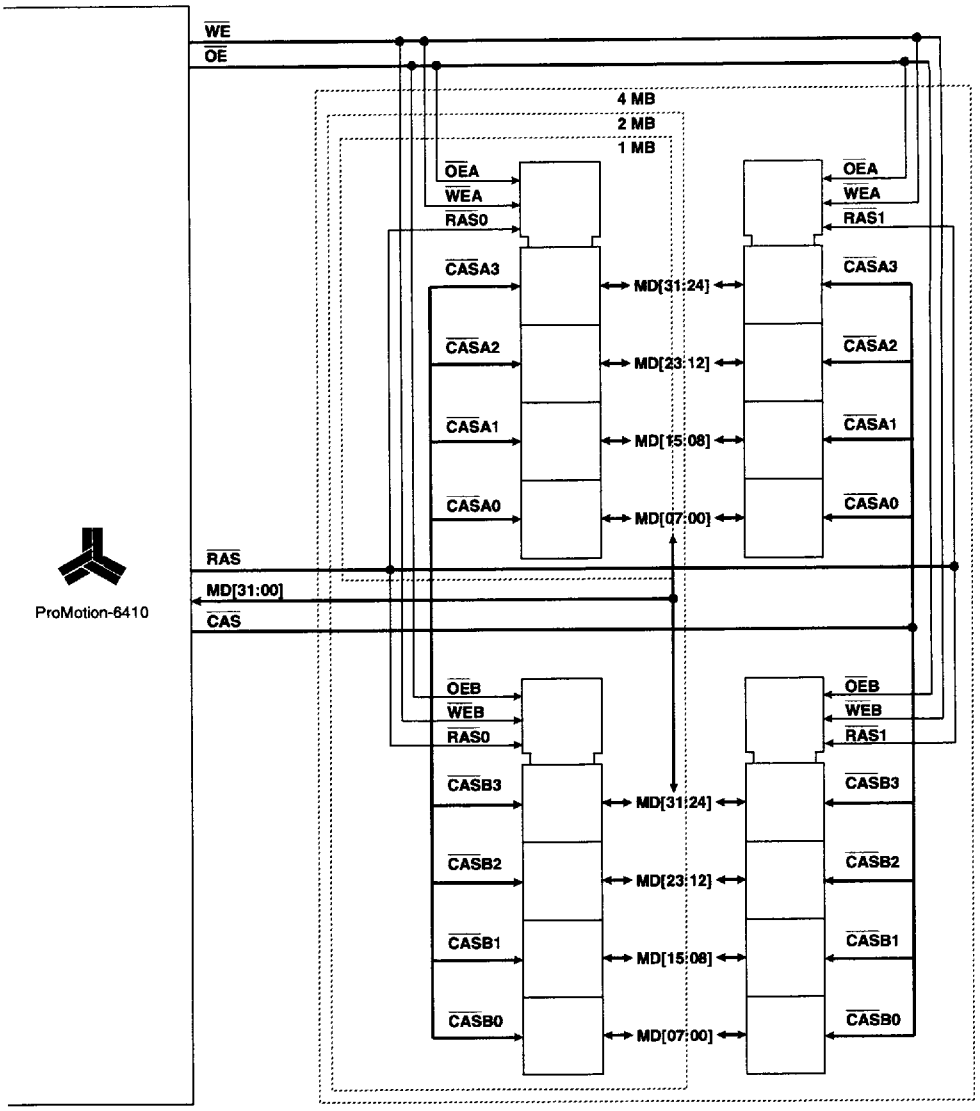
In PCI mode, ProMotion-6410 supports a dedicated address, data and Flash control interface for ROM BIOS. Refer to Figure 2.4.1, Glueless PCI/ROM interface.

In VL-bus mode, ProMotion-6410 decodes VGA BIOS addresses and drives a ROM enable signal. Address and data lines, as well as optional Flash control, are connected to the ISA bus. Refer to Figure 2.4.2, Glueless VL-bus/ROM interface.

2.6. DRAM interface

The ProMotion-6410 controls **1, 2, or 4 megabytes** of DRAM frame buffer memory. For 1MB and 2MB systems, 256K×4, ×8, or ×16 parts may be used. For 4MB systems, 256K×8 or ×16 may be used. Both dual-$\overline{CAS}$ and dual-$\overline{WE}$ organizations are supported; configuration strap MD[29] selects between the two modes.

Figure 2.6. Memory interface (default mode/multiple $\overline{CAS}$)



A **fully interleaved architecture** enables the ProMotion-6410 to read or write at a sustained rate of 64 bits every two cycles, matching the performance of more expensive 64-bit controllers. The chip also supports non-interleaved operation with 1MB of memory.

Programmable memory timing allows ProMotion-6410 to use standard speed DRAM or take advantage of Alliance Semiconductor's industry-leading fast DRAMs and other high-speed DRAMs.

2.7. Wideport DAC interface

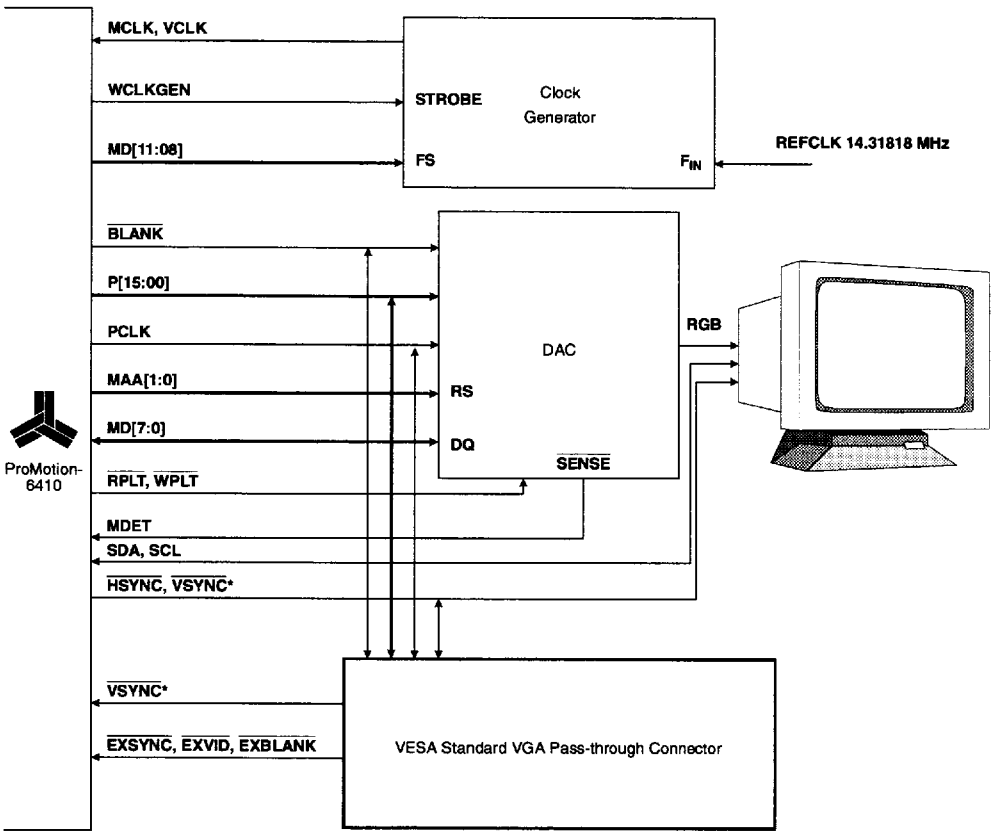
The ProMotion-6410 supports industry-standard pseudocolor and truecolor DACs with **8-bit or 16-bit pixel port** interface. Built-in scaling and color space conversion, as described in Section 2.2, gives outstanding motion video performance with a low-cost DAC.

The ProMotion-6410 controller can operate in single-edge or double-edge clocking mode. Refer to waveforms DAC timing: single-edge clocking mode on page 40 and DAC timing: double-edge clocking mode on page 41.

2.8. Feature connector interface

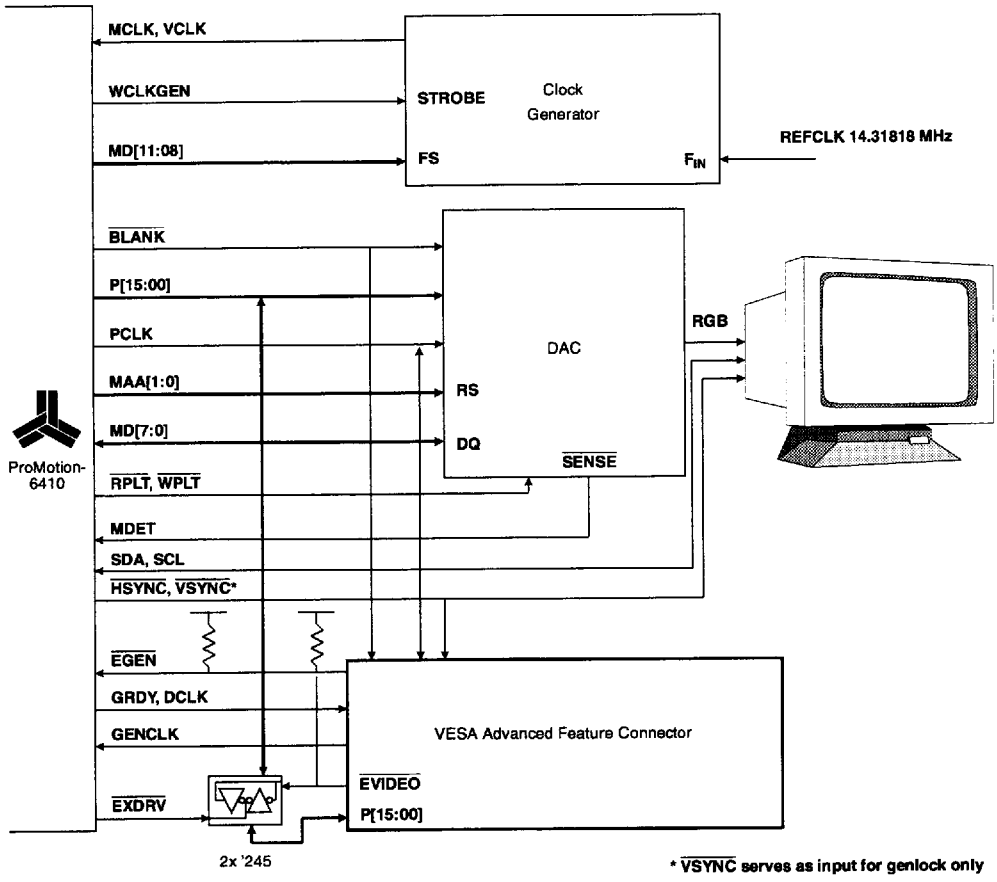
For interoperability with video capture and other multimedia cards, ProMotion-6410 offers two feature connector options, selectable by configuration strap MD[26]. In **VSVPC** mode, ProMotion-6410 connects to an industry-standard VGA Pass-through Connector: refer to Figure 2.8.1, VSVPC clock/DAC/feature connector. In **VAFC** mode, the chip supports the VESA Advanced Feature Connector standard, including 16-bit input and output. With the circuit shown in Figure 2.8.2, VAFC clock/DAC/feature connector, VAFC can be implemented without resorting to an expensive multiport DAC.

Figure 2.8.1. VSVPC clock/DAC/feature connector



* VSYNC serves as input for genlock only

Figure 2.8.2. VAFC clock/DAC/feature connector



2.9. DDC Support

ProMotion-6410 includes dedicated control pins for bi-directional DDC monitor connections. Using industry standard protocols, software can use DDC to read status and write configurations to monitors.

3. VGA registers

Table 3.1. VGA attribute controller registers

Register	I/O mapped port (hex)	Index (hex)	Memory-mapped offset (hex)	Bits	r/w
(Index)	3C0			6	r/w
Palette register 0	3C0	00		6	r/w
Palette register 1	3C0	01		6	r/w
Palette register 2	3C0	02		6	r/w
Palette register 3	3C0	03		6	r/w
Palette register 4	3C0	04		6	r/w
Palette register 5	3C0	05		6	r/w
Palette register 6	3C0	06		6	r/w
Palette register 7	3C0	07		6	r/w
Palette register 8	3C0	08		6	r/w
Palette register 9	3C0	09		6	r/w
Palette register 10	3C0	0A		6	r/w
Palette register 11	3C0	0B		6	r/w
Palette register 12	3C0	0C		6	r/w
Palette register 13	3C0	0D		6	r/w
Palette register 14	3C0	0E		6	r/w
Palette register 15	3C0	0F		6	r/w
Mode control	3C0	10		8	r/w
Overscan color	3C0	11		8	r/w
Color plane enable	3C0	12		6	r/w
Horizontal pixel panning	3C0	13		4	r/w
Color select register	3C0	14		4	r/w

Table 3.2. VGA general registers

Register	I/O mapped port (hex)	Index (hex)	Memory-mapped offset (hex)	Bits	r/w
Item select/miscellaneous output	3C2			8	w
	3CC			8	r
Feature control/vertical enable	3BA			4	w
	3CA			4	r
Input status 0	3C2			8	r
Input status 1	3BA			6	r

Table 3.3. VGA sequencer registers

Register	I/O mapped port (hex)	Index (hex)	Memory-mapped offset (hex)	Bits	r/w
Sequencer index	3C4			4	r/w
Reset	3C5	00		2	r/w
Clocking mode	3C5	01		6	r/w
Map mask	3C5	02		4	r/w
Character map select	3C5	03		6	r/w
Memory mode	3C5	04		4	r/w

Table 3.4. VGA graphics controller registers

Register	I/O mapped port (hex)	Index (hex)	Memory-mapped offset (hex)	Bits	r/w
Graphics index	3CE			4	r/w
Set/reset	3CF	00		4	r/w
Enable set/reset	3CF	01		4	r/w
Color compare	3CF	02		4	r/w
Data rotate	3CF	03		5	r/w
Read map select	3CF	04		2	r/w
Graphics mode	3CF	05		5	r/w
Miscellaneous	3CF	06		4	r/w
Color don't care	3CF	07		4	r/w
Bit mask	3CF	08		8	r/w

Table 3.5. VGA setup registers

Register	I/O mapped port (hex)	Index (hex)	Memory-mapped offset (hex)	Bits	r/w
Video subsystem enable	46E8			2	r/w
Setup option select	102			1	r/w

Table 3.6. VGA CRTC registers

Register	I/O mapped port (hex)	Index (hex)	Memory-mapped offset (hex)	Bits	r/w
CRTC index	3D4			6	r/w
Horizontal total	3D5	00		8	r/w
Horizontal display enable end	3D5	01		8	r/w
Horizontal blank start	3D5	02		8	r/w
Horizontal blank end	3D5	03		7	r/w
Horizontal retrace start	3D5	04		8	r/w
Horizontal retrace end	3D5	05		8	r/w

Table 3.6. VGA CRTC registers

Register	I/O mapped port (hex)	Index (hex)	Memory-mapped offset (hex)	Bits	r/w
Vertical total	3D5	06		8	r/w
Vertical overflow	3D5	07		8	r/w
Preset row scan	3D5	08		7	r/w
Maximum scan line	3D5	09		8	r/w
Block cursor start	3D5	0A		6	r/w
Block cursor end	3D5	0B		7	r/w
Serial start address	3D5	0C		16	r/w
Block cursor location	3D5	0E		16	r/w
Vertical retrace start	3D5	10		8	r/w
Vertical retrace end	3D5	11		8	r/w
Vertical display enable end	3D5	12		8	r/w
Serial offset	3D5	13		8	r/w
Underline location/dword mode	3D5	14		7	r/w
Vertical blank start	3D5	15		8	r/w
Vertical blank end	3D5	16		8	r/w
CRTC mode control register	3D5	17		8	r/w
Line compare	3D5	18		8	r/w
Readback latch data	3D5	22			r
Attribute index data	3D5	24		8	r

Table 3.7. VGA palette DAC registers

Register	I/O mapped port (hex)	Index (hex)	Memory-mapped offset (hex)	Bits	r/w
Palette DAC pel mask	3C6			8	r/w
Palette DAC read address	3C7			8	w
Palette DAC state	3C7			2	r
Palette DAC write address	3C8			8	r/w
Palette DAC data	3C9			8	r/w

4. ProMotion-6410 extended registers

Table 4.1. Extended setup registers

Register	I/O mapped port (hex)	Index (hex)	Memory-mapped offset (hex)	Bits	r/w
Unlock extended registers	3C5	10		8	r/w
Chip ID	3C5	11-19		8	r
Flat model base address	3C5	1A		8	r/w
Remap control	3C5	1B		6	r/w
Flat model control	3C5	1C		6	r/w
Extended status			1FC	15	r
Abort/DDC control			1FF	4	r/w

Table 4.2. Extended CRTC registers

Register	I/O mapped port (hex)	Index (hex)	Memory-mapped offset (hex)	Bits	r/w
Horizontal interlaced start	3D5	19		8	r/w
Vertical extended overflow	3D5	1A		7	r/w
Horizontal overflow	3D5	1B		5	r/w
Serial overflow	3D5	1C		8	r/w
Character clock adjust	3D5	1D		3	r/w

Table 4.3. Drawing engine registers

Register	I/O mapped port (hex)	Index (hex)	Memory-mapped offset (hex)	Bits	r/w
Clipping enable			030	3	r/w
Clipping boundary left			038	12	r/w
Clipping boundary top			03A	12	r/w
Clipping boundary right			03C	12	r/w
Clipping boundary bottom			03E	12	r/w
Drawing engine control			040	32	r/w
Raster operation			046	8	r/w
Byte mask			047	4	r/w
Pattern			048	64	r/w
Source location			050	32	r/w
Destination location			054	32	r/w
Source size			058	32	r/w
Foreground color			060	25	r/w
Background color/source transparency			064	25	r/w

Table 4.3. Drawing engine registers

Register	I/O mapped port (hex)	Index (hex)	Memory-mapped offset (hex)	Bits	r/w
DDA axial/diagonal step constant			070	32	r/w
DDA error term			074	16	r/w

Table 4.4. Motion video registers

Register	I/O mapped port (hex)	Index (hex)	Memory-mapped offset (hex)	Bits	r/w
vWindow control			082	16	r/w
vWindow data width			084	12	r/w
vWindow data pitch			086	12	r/w
vWindow left/top			088	32	r/w
vWindow right/bottom			08C	32	r/w
vWindow data base address			090	24	r/w
VAFC chromakey color			094	24	r/w
vWindow stretch factor horizontal			098	32	r/w
vWindow stretch factor vertical			09C	32	r/w

Table 4.5. Extended configuration registers

Register	I/O mapped port (hex)	Index (hex)	Memory-mapped offset (hex)	Bits	r/w
Serial control			080	6	r/w
Page offset			0C0	10	r/w
Aperture control			0C2	11	r/w
Display memory configuration			0C4	5	r/w
Output pixel data format			0C6	5	r/w
VGA override			0C8	14	r/w
Pin interface			0CA	3	r/w
Feature connector control			0CC	2	r/w
Generic feature connector control			0CD	6	r/w
VAFC control			0CE	3	r/w
Genlock control			0CF	8	r/w
DPMS control			0D0	2	r/w
Monitor interlace control			0D2	3	r/w
Pixel FIFO request point			0D4	24	r/w
External clock control			0D8	4	r/w
External signal timing			0D9	6	r/w
Internal control			0DA	1	r/w
Scratchpad registers	3C5	20–23		32	r/w

Table 4.6. Hardware cursor registers

Register	I/O mapped port (hex)	Index (hex)	Memory-mapped offset (hex)	Bits	r/w
H/W cursor control			140	32	r/w
H/W cursor pattern base address			144	12	r/w
H/W cursor display position			148	32	r/w
H/W cursor display offset			14C	16	r/w

Table 4.7. PCI configuration registers

Register	PCI I/O (hex)	Index (hex)	Offset (hex)	Bits	r/w
PCI vendor ID	00		180	8	r
PCI device ID	02		182	8	r
PCI command	04		184	16	r/w
PCI status	06		186	16	r
PCI revision ID	08		188	8	r
Class code	09		189	16	r/w
PCI base address	10		190	32	r/w
Expansion ROM base address	30		1B0	32	r/w
Interrupt line	3C		1BC	8	r/w
Interrupt pin	3D		1BD	8	r/w

5. Pin description

Table 5.1. PCI-bus host interface

Signal name	I/O	Drive	Description
IDSEL	I		Host address high byte is zero.
AD[31:00]	I/O	8 mA TS	Host address/data bus.
C/$\overline{BE}$[3:0]	I		Command/byte enable.
RST	I		System reset.
CLK	I		PCI clock.
$\overline{ROMWR}$	O	4 mA	ROM write. Used to write a Flash EPROM. Refer to the section ROM BIOS interface on page 5 for more information on Flash EPROM.
PAR	I/O	8 mA	Parity. ProMotion-6410 computes and drives parity for all host reads.
$\overline{FRAME}$	I		Cycle frame. Asserted by the host for the duration of an access.
$\overline{IRDY}$	I	8 mA TS	Initiator ready. Asserted by the host when it is ready to transmit or receive data.
$\overline{TRDY}$	O	8 mA TS	Target ready. Asserted by ProMotion-6410 when it is ready to transmit or receive data.
$\overline{DEVSEL}$	O	8 mA	Local device. Asserted by ProMotion-6410 when it identifies itself as target of a PCI-bus cycle.
$\overline{IRQA}$	O	8 mA	Interrupt request.

Table 5.2. VL-bus host interface

Signal name	I/O	Drive	Description
ADR[31:02]	I		Host address bus, bits 31:02.
DAT[31:00]	I/O	8 mA TS	Host data bus.
$\overline{BE}$[3:0]	I		Byte enable. Selects which bytes of DAT are read or written.
$\overline{RESET}$	I		System reset.
LCLK	I		VL-bus clock.
M/$\overline{IO}$	I		Memory/IO cycle select.
W/$\overline{R}$	I		Write/Read cycle select.
$\overline{ADS}$	I		Address strobe. Indicates that VL-bus address is valid.
$\overline{RDYRTN}$	I		Ready return. Asserted by the host to terminate the current cycle.
$\overline{LRDY}$	O	8 mA TS	Local ready. Asserted by ProMotion-6410 when cycle has completed.
$\overline{LDEV}$	O	8 mA TS	Local device. Asserted by ProMotion-6410 when it identifies itself as target of a VL-bus cycle.

Table 5.3. DRAM interface

Signal name	I/O	Drive	Description
MD[31:0]	I/O	4 mA	DRAM data.
MAA[8:0]	O	8 mA	DRAM address, bank A.
MAB[8:0]	O	8 mA	DRAM address, bank B.
$\overline{RAS}$[1:0]	O	8 mA	Row address strobe. In 4MB systems, RAS[0] selects the first two 1MB banks and RAS[1] selects the second two 1MB banks. In 2MB systems, RAS[1] may be configured as a second copy of $\overline{RAS}$[0].
$\overline{CASA}$[3:0]/$\overline{WEA}$[3:0]	O	8 mA	Byte-wise $\overline{CAS}$/$\overline{WE}$ control, bank A. In default mode, drives per-byte $\overline{CAS}$ lines. In multiple $\overline{WE}$ mode, drives per-byte $\overline{WE}$ lines.
$\overline{CASB}$[3:0]/$\overline{WEB}$[3:0]	O	8 mA	Byte-wise $\overline{CAS}$/$\overline{WE}$ control, bank B In default mode, drives per-byte $\overline{CAS}$ lines. In multiple $\overline{WE}$ mode, drives per-byte $\overline{WE}$ lines.
$\overline{OEA}$	O	8 mA	Output enable, bank A.
$\overline{OEB}$	O	8 mA	Output enable, bank B.
$\overline{WEA}$/$\overline{CASA}$	O	8 mA	Bank wise $\overline{WE}$/$\overline{CAS}$ control, bank A. In default mode, drives bank A $\overline{WE}$. In multiple $\overline{WE}$ mode, drives bank A $\overline{CAS}$.
$\overline{WEB}$/$\overline{CASB}$	O	8 mA	Bank wise $\overline{WE}$/$\overline{CAS}$ control, bank B. In default mode, drives bank B $\overline{WE}$. In multiple $\overline{WE}$ mode, drives bank B $\overline{CAS}$.

Table 5.4. Clock generator interface

Signal name	I/O	Drive	Description
MCLK	I		Memory clock in.
VCLK	I		Video clock in. Pixel data PCLK is generated from VCLK. See below.
WCLKGEN	O	4 mA	Write clock generator. Strobe frequency select data from MD[11:08]

Table 5.5. DAC/monitor interface

Signal name	I/O	Drive	Description
P[15:00]	O	8 mA TS	Pixel data to DAC. Eight-bit DACs use P[7:0] only.
PCLK	O	8 mA TS	Pixel clock to DAC. A phase delayed or divided-down copy of VCLK depending on the status of clocking mode register, 3C5.1.
RPLT	O	4 mA	DAC register read strobe.
$\overline{\text{WPLT}}$	O	4 mA	DAC register write strobe.
$\overline{\text{HSYNC}}$	O	12 mA TS	Horizontal sync to monitor.
$\overline{\text{VSYNC}}$	I/O	12 mA	Vertical sync to monitor. In genlock mode, vertical sync input from feature connector.
$\overline{\text{BLANK}}$	O	8 mA TS	Blank signal to DAC.
MDET	I		Monitor sense from DAC.
$\overline{\text{EGEN}}$	I		Enable GENCLK to drive in place of VCLK.
GENCLK	I		Genlock clock from feature connector.
SDA*	I/O	8 ma TS	DDC data.
SCL*	I/O	8 mA TS	DDC clock.

*Rev. D and later.

Table 5.6. Feature connector interface VSVPC mode

Signal name	I/O	Drive	Description
$\overline{\text{EXVID}}$	I		External video. Places ProMotion-6410 P[15:0] lines in high-impedance mode, so external device can drive DAC pixel data bus.
$\overline{\text{EXPCLK}}$	I		External clock. Places ProMotion-6410 PCLK in high-impedance mode, so external device can drive DAC pixel clock.
$\overline{\text{EXSYNC}}$	I		External sync. Places ProMotion-6410 $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$, and $\overline{\text{BLANK}}$ signals in high-impedance mode, so external devices can drive them.

Table 5.7. Feature connector interface VAFC mode

Signal name	I/O	Drive	Description
$\overline{\text{EXDRV}}$	O		External pixel driver enable.
DCLK	O	4 mA	Dot clock. Equal to PCLK or PCLK/2 depending on state of VAFC control register.
GRDY	O	4 mA	Graphics ready. Signals that external pixel has been accepted.

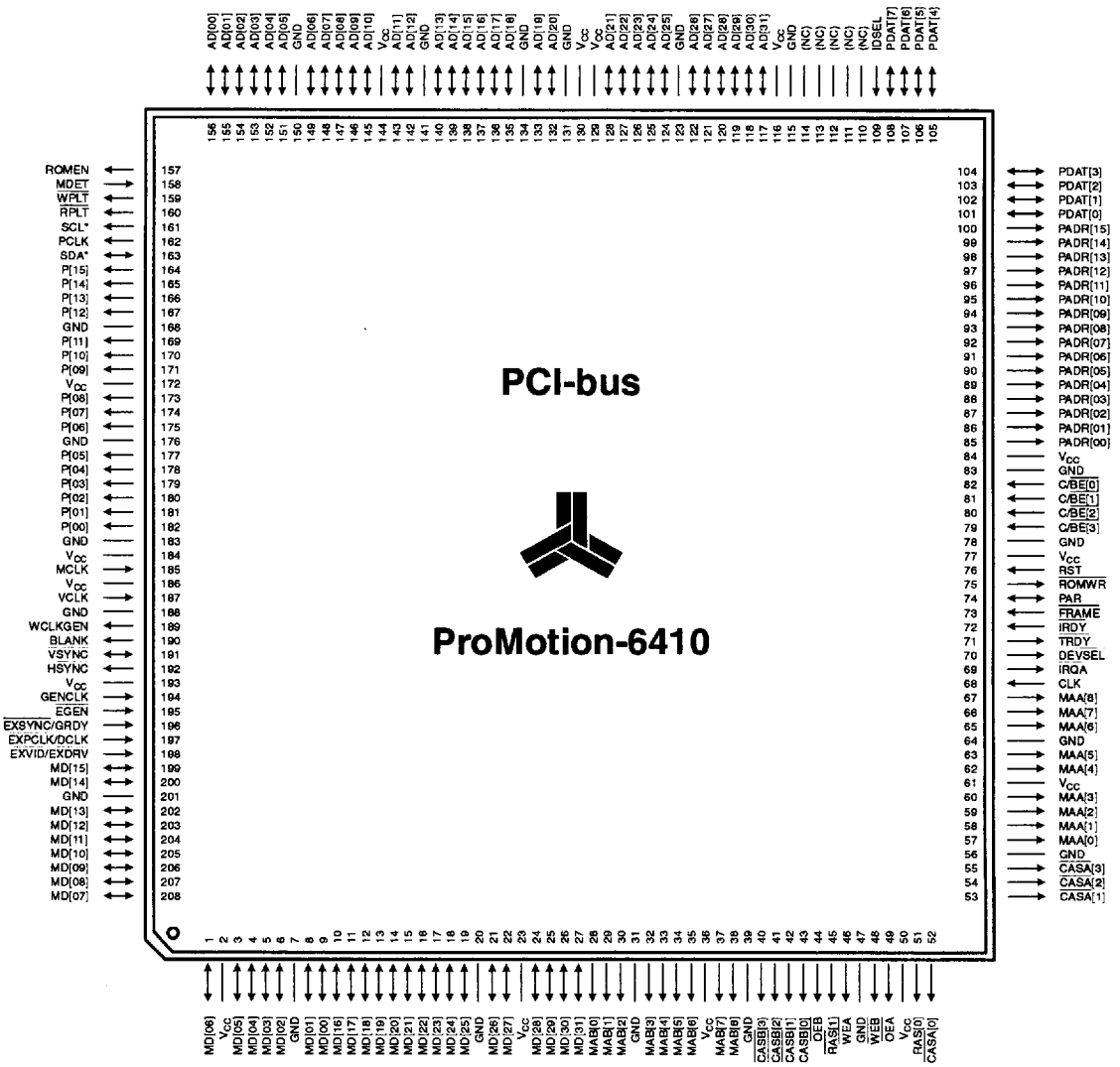
Table 5.8. ROM BIOS interface

Signal name	I/O	Drive	Description
PADR[15:0]	O	4 mA	Private ROM address bus (PCI only).
PDAT[7:0]	I/O	4 mA	Private ROM data bus (PCI only).
$\overline{\text{ROMEN}}$	O	4 mA	External ROM enable (all modes).

Table 5.9. Power/ground pins

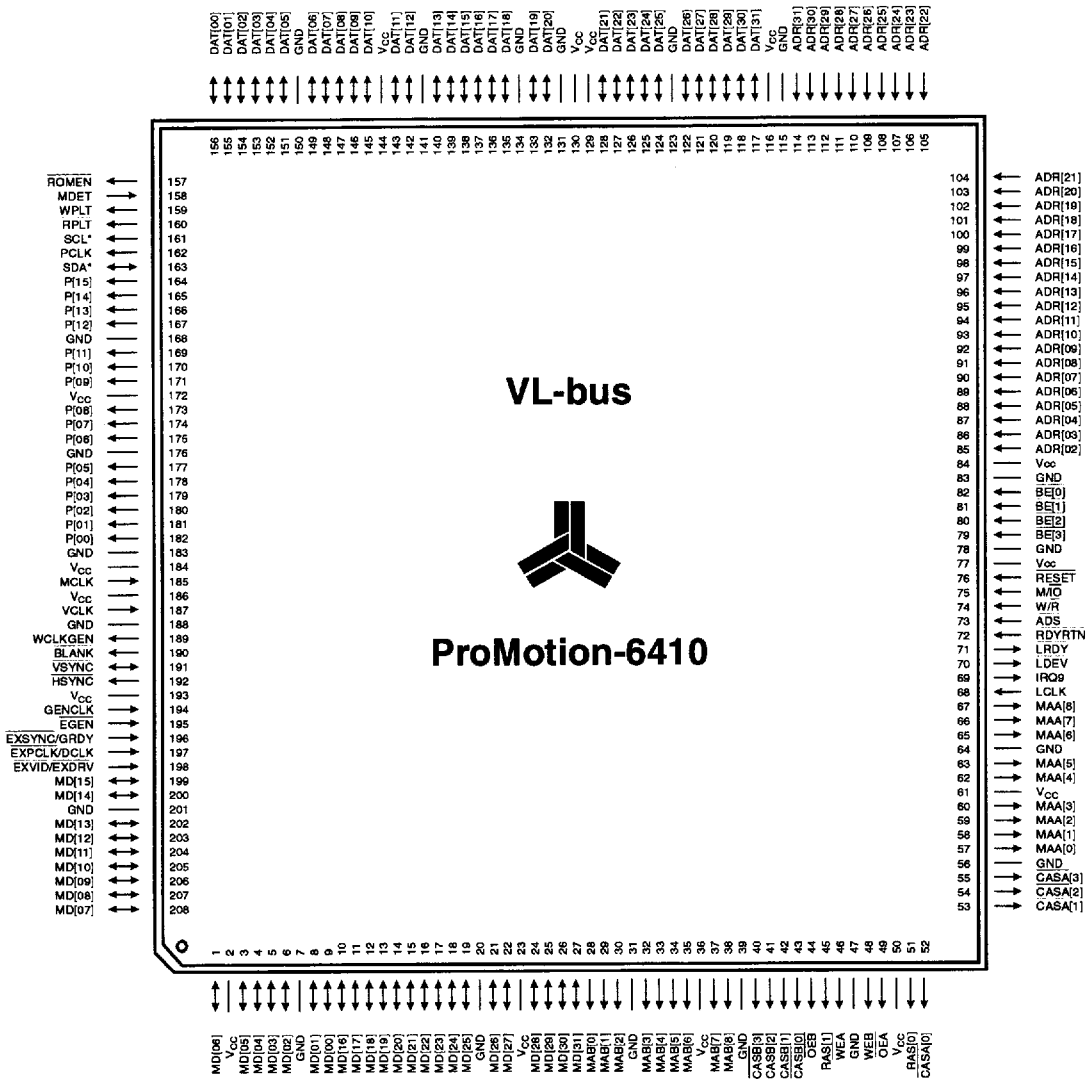
Signal name	I/O	Drive	Description
V_{CC}			Power.
GND			Ground.

Figure 5.1. PCI-bus pin diagram



*Rev D and later.

Figure 5.2. VL-bus pin diagram



*Rev D and later.

6. Configuration straps

Signal name	MD	Description	Offset [bit]	r/w[1]
$\overline{\text{MAPOUT}}$	31	Pull down to map out ROM.	0C2[3]	r/w
$\overline{\text{INTLV}}$	30	Pull down for interleaved display memory.	0C4[0]	r/w
$\overline{\text{MULTWE}}$	29	Pull down for multiple-$\overline{\text{WE}}$ DRAM array. Default is multiple-$\overline{\text{CAS}}$ array.	0C4[4]	r/w
-	28	Reserved. Do not connect.	0C6[2]	-
VL/$\overline{\text{PCI}}$	27	Pull down for PCI configuration. Default is VL-bus mode.	0CA[0]	r
$\overline{\text{DAC16}}$	26	Pull down for 16-bit pixel port. Default is 8-bit pixel port. $\overline{\text{DAC16}}$ must be configured by the hardware strap. It cannot be overridden by BIOS software.	0CA[1]	r
$\overline{\text{LDEVTS}}$	25	Pull down for wired-OR $\overline{\text{LDEV}}$. Default is dedicated $\overline{\text{LDEV}}$. This strap must be pulled low for PCI configurations. $\overline{\text{LDEVTS}}$ must be configured by the hardware strap. It cannot be overridden by BIOS software.	0CA[2]	r
$\overline{\text{SEL3C3}}$	24	Pull down for video subsystem 3C3.	0C2[0]	r/w
$\overline{\text{DUALRAS}}$	23	Pull down to duplicate $\overline{\text{RAS}}$ ($\overline{\text{RAS}}$1 = $\overline{\text{RAS}}$0, max 2MB RAM). Default is separate $\overline{\text{RAS}}$ (max 4MB RAM).	0C4[6]	r/w
$\overline{\text{FASTRAS}}$	22	Pull down for extended $\overline{\text{RAS}}$ (fast $\overline{\text{RAS}}$ disable). Default is fast $\overline{\text{RAS}}$ enabled.[2]	0C4[1]	r/w
INTPIN	11	Pull down to set PCI interrupt pin configuration register to read back value of 1. Default reads value of 0.	1BD[0]	r

[1] w in this column indicates hardware may be overridden by BIOS.

[2] Alliance recommends extended $\overline{\text{RAS}}$ for MCLK rates >50MHz. Fast RAS is recommended for MCLK rates <=50MHz, with DRAM access 70ns or faster. Refer to Display memory timing: read/write on page 37.

7. Electrical characteristics

Table 7.1. Absolute maximum ratings

Symbol	Parameter	Rating	Unit
T_a	Ambient temperature under load	0 to 70	° C
T_{stg}	Storage temperature	–65 to +150	° C
V_{IN}	Voltage on any pin	–0.5 to +6.5	Volts
P_D	Operating power dissipation	1.5	Watts
V_a	Power supply voltage	7.0	Volts
I_{out}	DC output current (per pin)	20	mA
	Injection current (latch up testing)	100	mA

NOTE: Stresses greater than those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 7.2. Recommended operating conditions

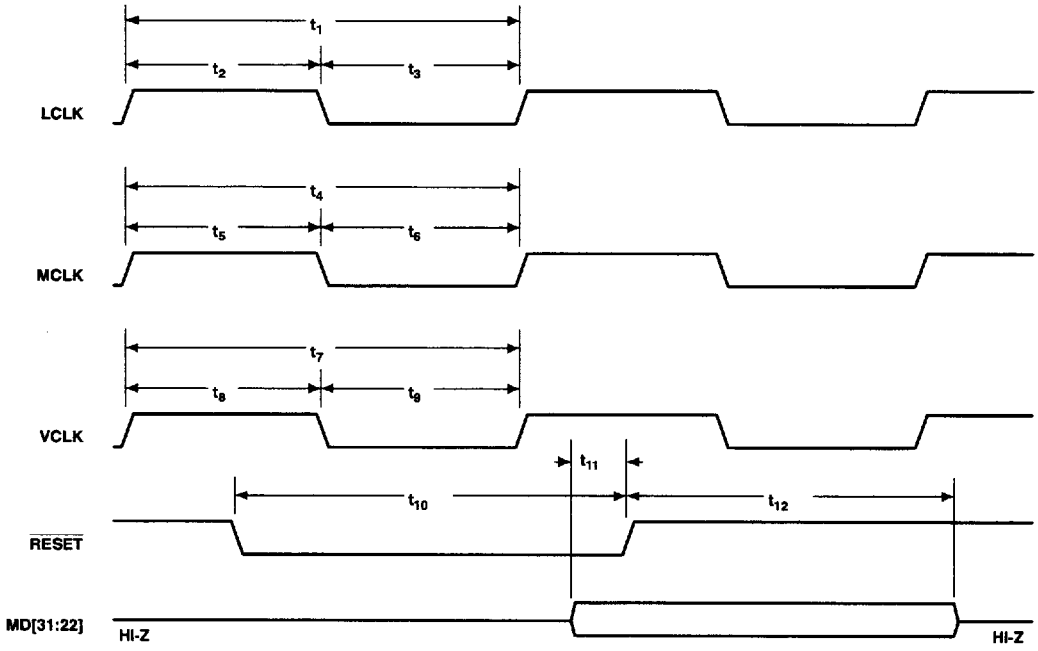
Symbol	Parameter	Test Conditions	Min	Max	Unit
V_{CC}	Power supply voltage	Normal operation	4.75	5.25	Volts
V_{IL}	Input low voltage		0	0.8	Volts
V_{IH}	Input high voltage		2.0	V_{CC} +0.5	Volts
V_{OL}	Output low voltage	I_{OL} = 4 mA		0.4	Volts
V_{OH}	Output high voltage	I_{OH} = 400 µA	2.4		Volts
I_{CC}	Supply current	V_{CC} Nominal		TBD	mA
I_{IH}	Input high current	$V_{IL} = V_{CC}$		10	µA
I_{IL}	Input low current	V_{CC} = 5.25 V, V_{IL} = –0.5 V	–10		µA
I_{OZ}	Input leakage	$0 < V_{IN} < V_{CC}$	–10	10	µA
C_{IN}	Input capacitance			10	pF
C_{OUT}	Output capacitance			10	pF

8. AC timing

8.1. Clock and reset timing

Waveform 8.1. Clock and reset timing

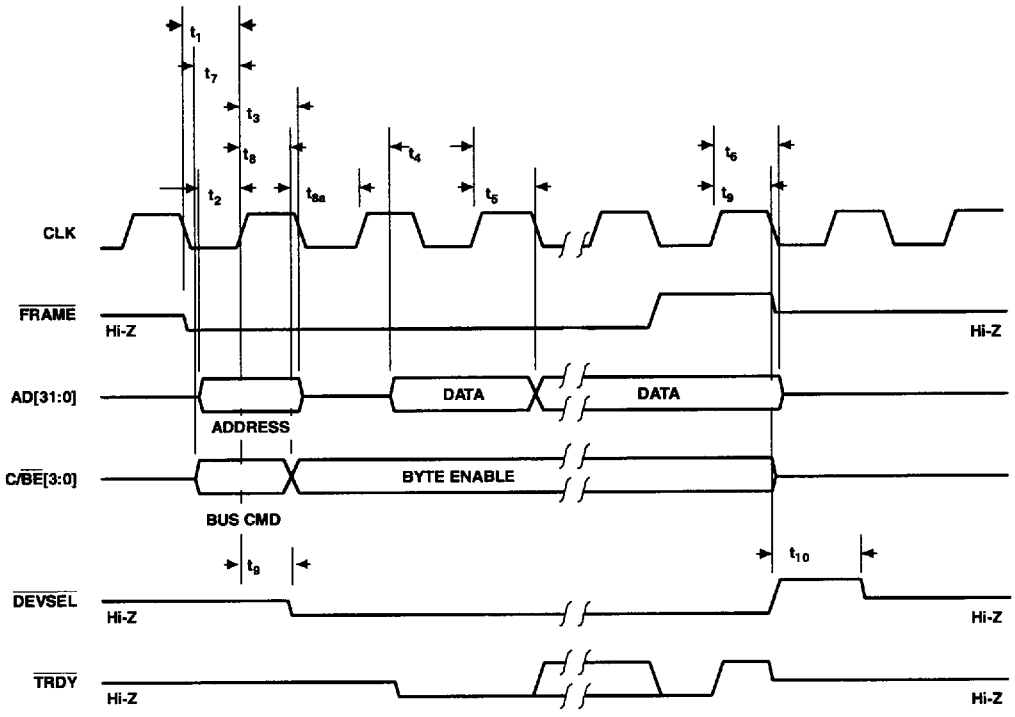
Symbol	Parameter	Min	Max	Unit
t_1	LCLK period	20		ns
t_2	LCLK high period	8		ns
t_3	LCLK low period	8		ns
t_4	MCLK period	18		ns
t_5	MCLK high period	7		ns
t_6	MCLK low period	7		ns
t_7	VCLK period	13		ns
t_8	VCLK high period	5		ns
t_9	VCLK low period	5		ns
t_{10}	$\overline{\text{RESET}}$ pulse width	400		ns
t_{11}	MD strap setup to $\overline{\text{RESET}}$ inactive	10		ns
t_{12}	MD strap hold from $\overline{\text{RESET}}$ inactive	5		ns



8.2. Host interface timing

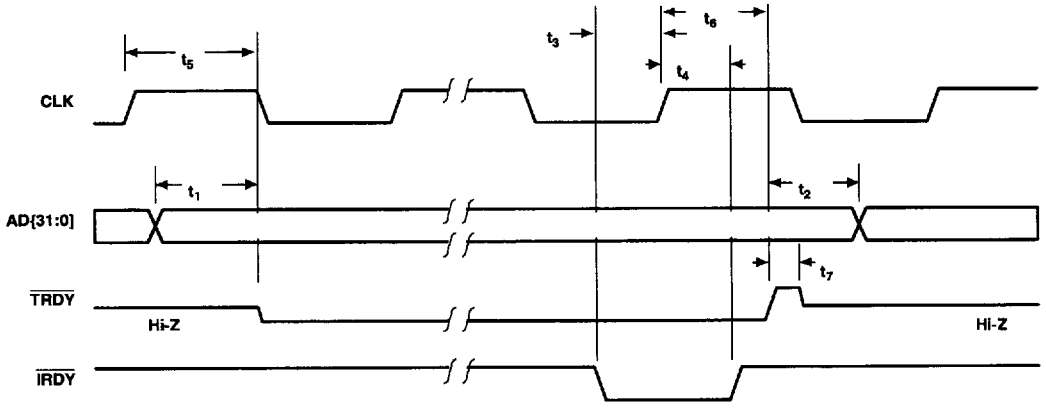
Waveform 8.2.1. PCI timing: FRAME, DEVSEL, AD[31:0], C/BE[3:0]

Symbol	Parameter	Min	Max	Unit
t_1	FRAME setup to CLK	7		ns
t_2	AD[31:0] (address) setup to CLK	7		ns
t_3	AD[31:0] (address) hold from CLK	0		ns
t_4	AD[31:0] (data) setup to CLK	7		ns
t_5	AD[31:0] (data) hold from CLK	0		ns
t_6	AD[31:0] C/BE[3:0] Hi-Z from CLK	0	28	ns
t_7	C/BE[3:0] (bus CMD) setup to CLK	7		ns
t_8	C/BE[31:0] (bus CMD) hold from CLK	0		ns
t_{8a}	C/BE[3:0] (byte enable) setup to CLK	7		ns
t_9	DEVSEL delay from CLK		15	ns
t_{10}	DEVSEL high before Hi-Z	1 CLK		ns



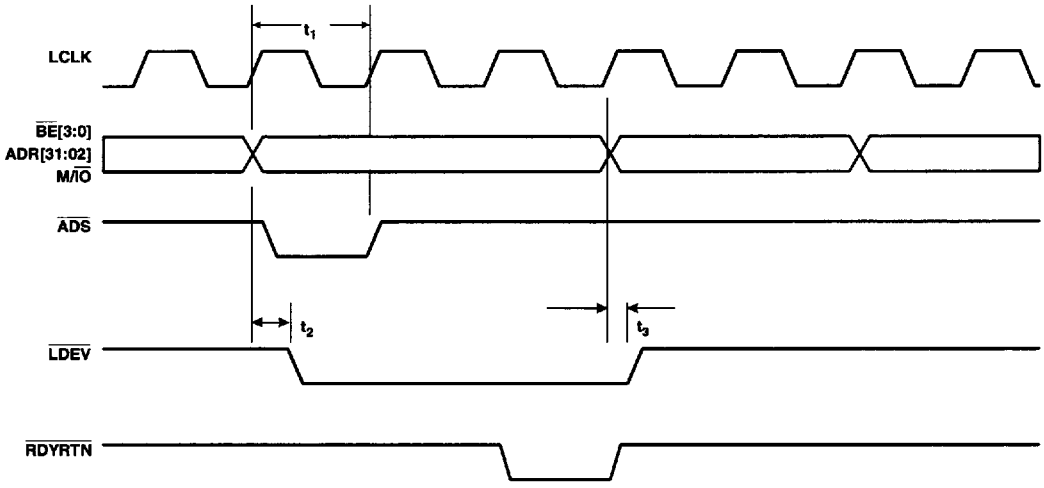
Waveform 8.2.2. PCI timing; $\overline{TRDY}$, $\overline{IRDY}$, read data

Symbol	Parameter	Min	Max	Unit
t_1	Read data setup to $\overline{TRDY}$ active	7		ns
t_2	Read data hold from $\overline{TRDY}$ inactive	0		ns
t_3	$\overline{IRDY}$ setup to CLK	7		ns
t_4	$\overline{IRDY}$ hold from CLK	0		ns
t_5	$\overline{TRDY}$ active delay from CLK		15	ns
t_6	$\overline{TRDY}$ inactive delay from CLK		15	ns
t_7	$\overline{TRDY}$ high before Hi-Z	1 CLK		ns



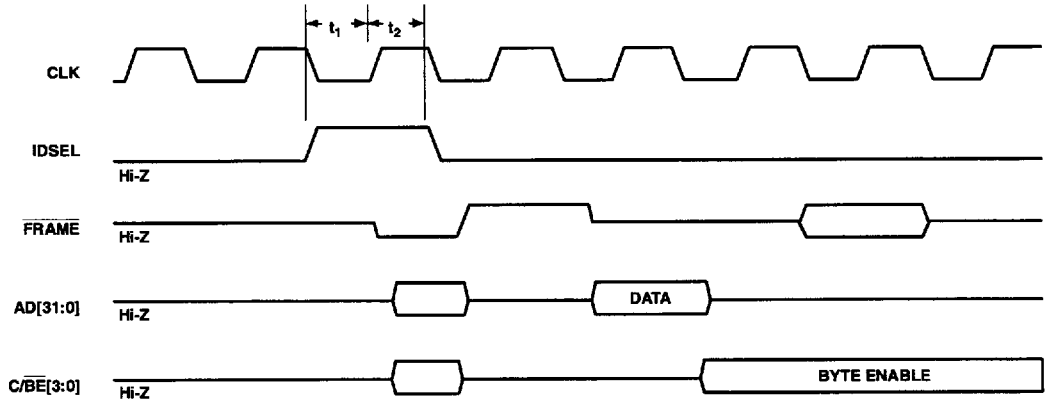
Waveform 8.2.3. VL-bus timing: $\overline{ADS}$, $\overline{LDEV}$

Symbol	Parameter	Min	Max	Unit
t_1	Address, status, $\overline{ADS}$ setup to LCLK	8		ns
t_2	$\overline{LDEV}$ active delay from address, status		15	ns
t_3	$\overline{LDEV}$ inactive delay from address, status		15	ns



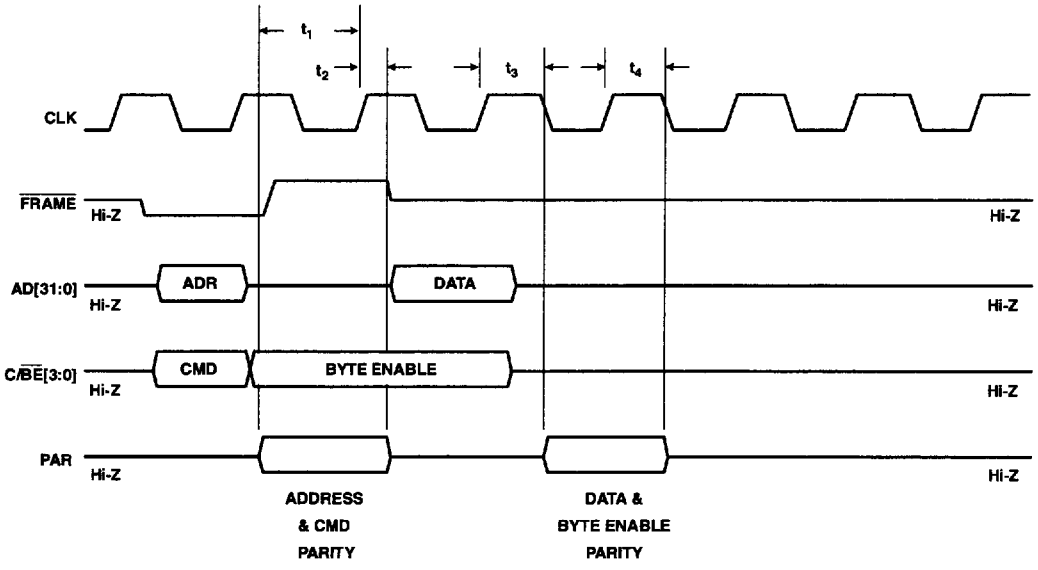
Waveform 8.2.4. PCI timing: IDSEL

Symbol	Parameter	Min	Max	Unit
t_1	IDSEL setup to CLK		15	ns
t_2	IDSEL hold from CLK		15	ns



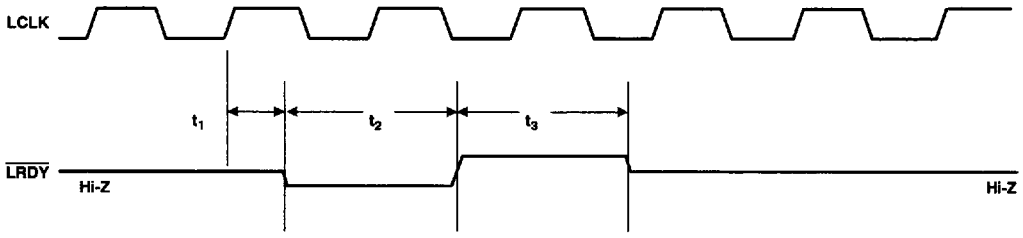
Waveform 8.2.5. PCI timing: PAR

Symbol	Parameter	Min	Max	Unit
t_1	PAR setup to CLK as input	7		ns
t_2	PAR hold from CLK as input	0		ns
t_3	PAR delay from CLK as output	7		ns
t_4	PAR hold from CLK as output	0		ns



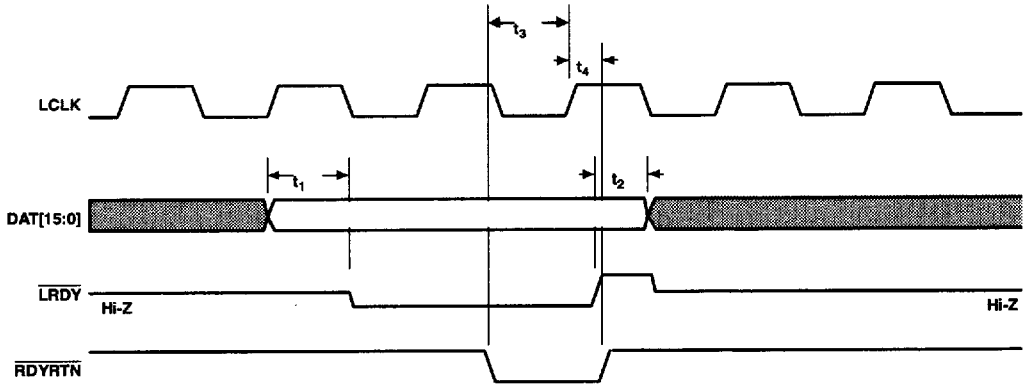
Waveform 8.2.6. VL-bus timing: $\overline{\text{LRDY}}$ delay

Symbol	Parameter	Min	Max	Unit
t_1	$\overline{\text{LRDY}}$ active delay from LCLK		14	ns
t_2	$\overline{\text{LRDY}}$ inactive delay from LCLK		14	ns
t_3	$\overline{\text{LRDY}}$ HIGH		LCLK/2	ns



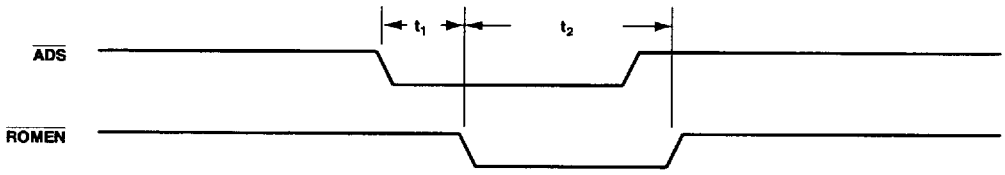
Waveform 8.2.7. VL-bus timing: read data

Symbol	Parameter	Min	Max	Unit
t_1	Read data setup to $\overline{\text{LRDY}}$ active	0		ns
t_2	Read data hold from $\overline{\text{LRDY}}$ inactive	12		ns
t_3	$\overline{\text{RDYRTN}}$ setup to LCLK	8		ns
t_4	$\overline{\text{RDYRTN}}$ hold from LCLK	5		ns



Waveform 8.2.8. VL-bus timing: BIOS ROM read

Symbol	Parameter	Min	Max	Unit
t_1	$\overline{\text{ADS}}$ low to $\overline{\text{ROMEN}}$ low		2 LCLK	ns
t_2	$\overline{\text{ROMEN}}$ pulse width	500		ns

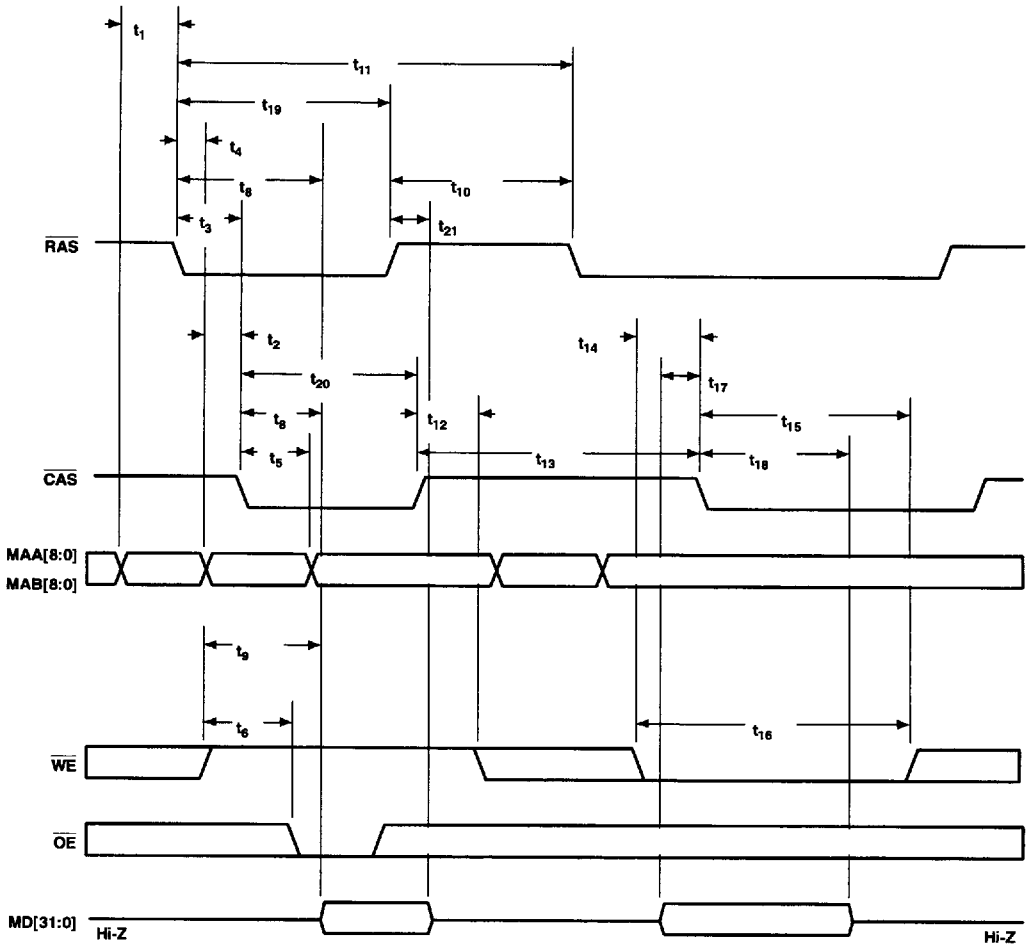


8.3. Display memory timing

Waveform 8.3.1. Display memory timing: read/write

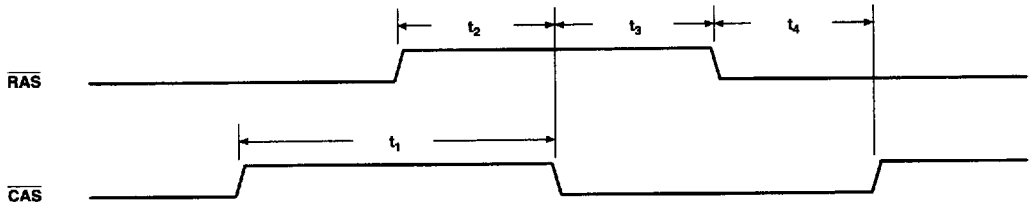
Symbol	Std. Symbol	Parameter	Min	Max	Unit
t_1	t_{ASR}	MA setup to $\overline{RAS}$ active (fast RAS)	1.5 MCLK		ns
		MA setup to $\overline{RAS}$ active (ext. RAS)	2 MCLK		ns
t_2	t_{ASC}	MA setup to $\overline{CAS}$ active	1 MCLK		ns
t_3	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ delay (fast RAS)	2.5 MCLK		ns
		$\overline{RAS}$ to $\overline{CAS}$ delay (ext. RAS)	3 MCLK		ns
t_4	t_{RAH}	Row address hold from $\overline{RAS}$ active (fast RAS)	1.5 MCLK		ns
		Row address hold from $\overline{RAS}$ active (ext. RAS)	2 MCLK		ns
t_5	t_{CAH}	Column address hold from $\overline{CAS}$ active	1 MCLK		ns
t_6		$\overline{WE}$ inactive to $\overline{OE}$ active	1 MCLK		ns
t_7	t_{RAC}	Data valid from $\overline{RAS}$ (fast $\overline{RAS}$)		3.5 MCLK	ns
		Data valid from $\overline{RAS}$ (ext. $\overline{RAS}$)		4 MCLK	ns
t_8	t_{CAC}	Data valid from $\overline{CAS}$ active		1 MCLK	ns
t_9	t_{AA}	Data valid from column address valid		2 MCLK	ns
t_{10}	t_{RP}	$\overline{RAS}$ precharge (fast $\overline{RAS}$)	2.5 MCLK		ns
		$\overline{RAS}$ precharge (ext. $\overline{RAS}$)	3 MCLK		ns
t_{11}	t_{RC}	Random cycle (fast $\overline{RAS}$)	6 MCLK		ns
		Random cycle (ext. $\overline{RAS}$)	7 MCLK		ns
t_{12}	t_{RCH}	Read command hold from $\overline{CAS}$ high	1 MCLK		ns
t_{13}	t_{CP}	$\overline{CAS}$ precharge	1 MCLK		ns
t_{14}	t_{CWL}	$\overline{WE}$ active setup to $\overline{CAS}$ active	0 MCLK		ns
t_{15}	t_{WCH}	$\overline{WE}$ active hold from $\overline{CAS}$ active	1 MCLK		ns
t_{16}	t_{WP}	$\overline{WE}$ active pulse width	1 MCLK		ns
t_{17}	t_{DS}	Write data setup to $\overline{CAS}$ active	0.5 MCLK		ns
t_{18}	t_{DH}	Write data hold from $\overline{CAS}$ active	0.5 MCLK		ns
t_{19}	t_{RAS}	$\overline{RAS}$ pulse width low (fast $\overline{RAS}$)	3.5 MCLK		ns
		$\overline{RAS}$ pulse width low (ext. $\overline{RAS}$)	4 MCLK		ns
t_{20}	t_{CAS}	$\overline{CAS}$ pulse width low	1 MCLK		ns
t_{21}	t_{PC}	Page mode cycle time	2 MCLK		ns

Waveform 8.3.1. Display memory timing: read/write



Waveform 8.3.2. Display memory timing: $\overline{CAS}$ before $\overline{RAS}$ refresh

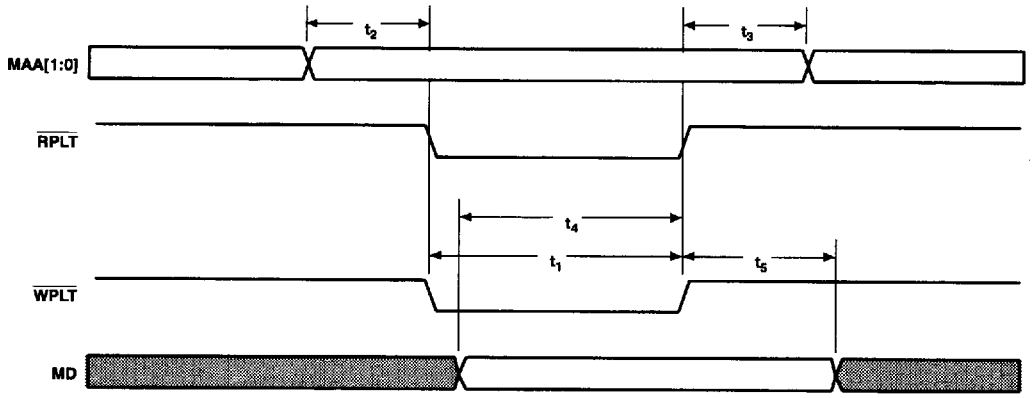
Symbol	Std. Symbol	Parameter	Min	Max	Unit
t_1	t_{CPN}	$\overline{CAS}$ precharge time	1 MCLK		ns
t_2	t_{RPC}	$\overline{RAS}$ high to $\overline{CAS}$ low precharge time	1 MCLK		ns
t_3	t_{CSR}	$\overline{CAS}$ before $\overline{RAS}$ setup time	1.5 MCLK		ns
t_4	t_{CHR}	$\overline{CAS}$ before $\overline{RAS}$ hold time	3.5 MCLK		ns



8.4. DAC/feature connector timing

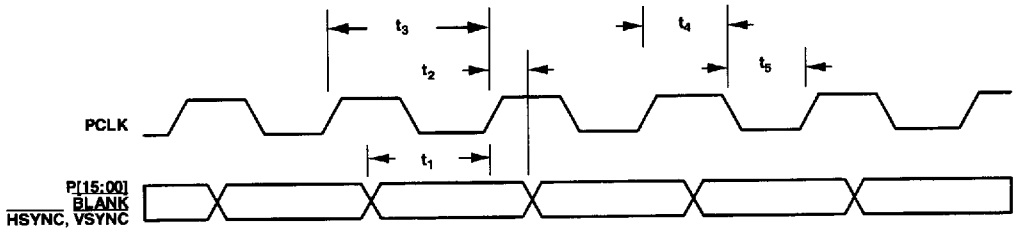
Waveform 8.4.1. DAC timing: register access

Symbol	Parameter	Min	Max	Unit
t_1	$\overline{RPLT}$, $\overline{WPLT}$ pulse width	4 MCLK		ns
t_2	Address setup	2 MCLK		ns
t_3	Address hold	2 MCLK		ns
t_4	Data setup	3.5 MCLK		ns
t_5	Data hold	2.5 MCLK		ns



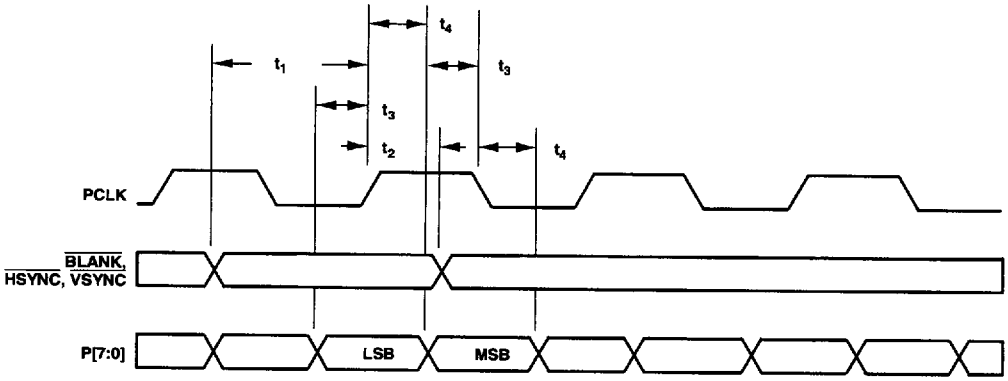
Waveform 8.4.2. DAC timing: single-edge clocking mode

Symbol	Parameter	Min	Max	Unit
t_1	P[15:00], $\overline{\text{BLANK}}$, $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$ setup time	4		ns
t_2	P[15:00], $\overline{\text{BLANK}}$, $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$ hold time	4		ns
t_3	PCLK period	12		ns
t_4	PCLK high time	5		ns
t_5	PCLK low time	5		ns



Waveform 8.4.3. DAC timing: double-edge clocking mode

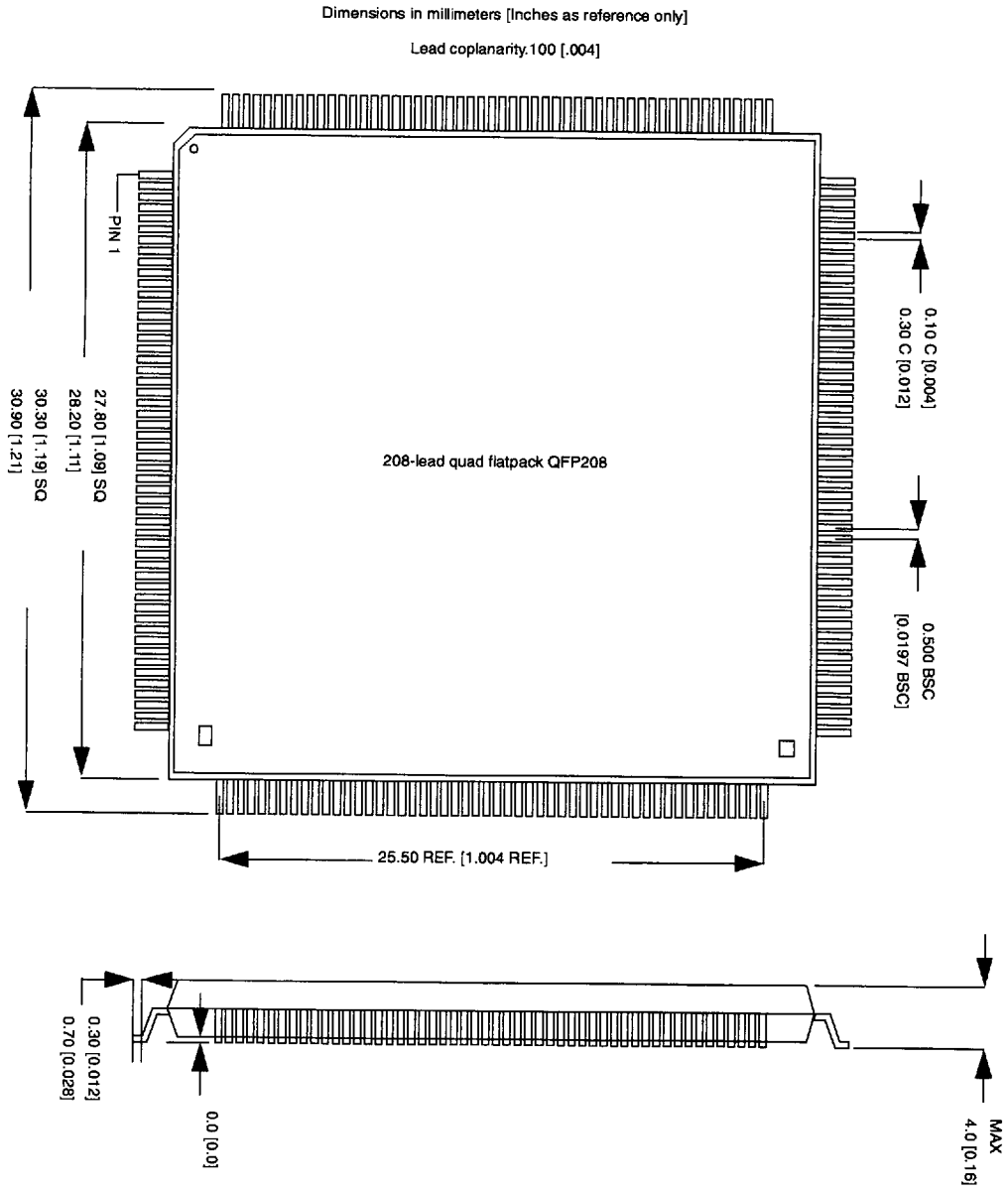
Symbol	Parameter	Min	Max	Unit
t_1	$\overline{\text{BLANK}}$, $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$ setup time	4		ns
t_2	$\overline{\text{BLANK}}$, $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$ hold time	4		ns
t_3	P[7:0] setup time	4		ns
t_4	P[7:0] hold time	4		ns



8.5. Test conditions

Pin name	Capacitive load	Unit
$\overline{\text{BLANK}}$, $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$, PCLK	30	pF
P[15:00]	40	pF
$\overline{\text{RPLT}}$, $\overline{\text{WPLT}}$, WCLKGEN	50	pF
MAA[8:0], MAB[8:0]	60	pF
$\overline{\text{CASA}}$, $\overline{\text{CASB}}$, $\overline{\text{OEA}}$, $\overline{\text{OEB}}$	40	pF
$\overline{\text{RAS}}$[1:0], $\overline{\text{WEA}}$, $\overline{\text{WEB}}$	80	pF
MD[31:00]	30	pF
DAT[31:0], IRQ, M/$\overline{\text{IO}}$, $\overline{\text{LRDY}}$, W/$\overline{\text{R}}$	75	pF
$\overline{\text{LDEV}}$	20	pF
$\overline{\text{ROMEN}}$	40	pF

9. Physical dimensions



9. Physical dimensions